Electronic Design®

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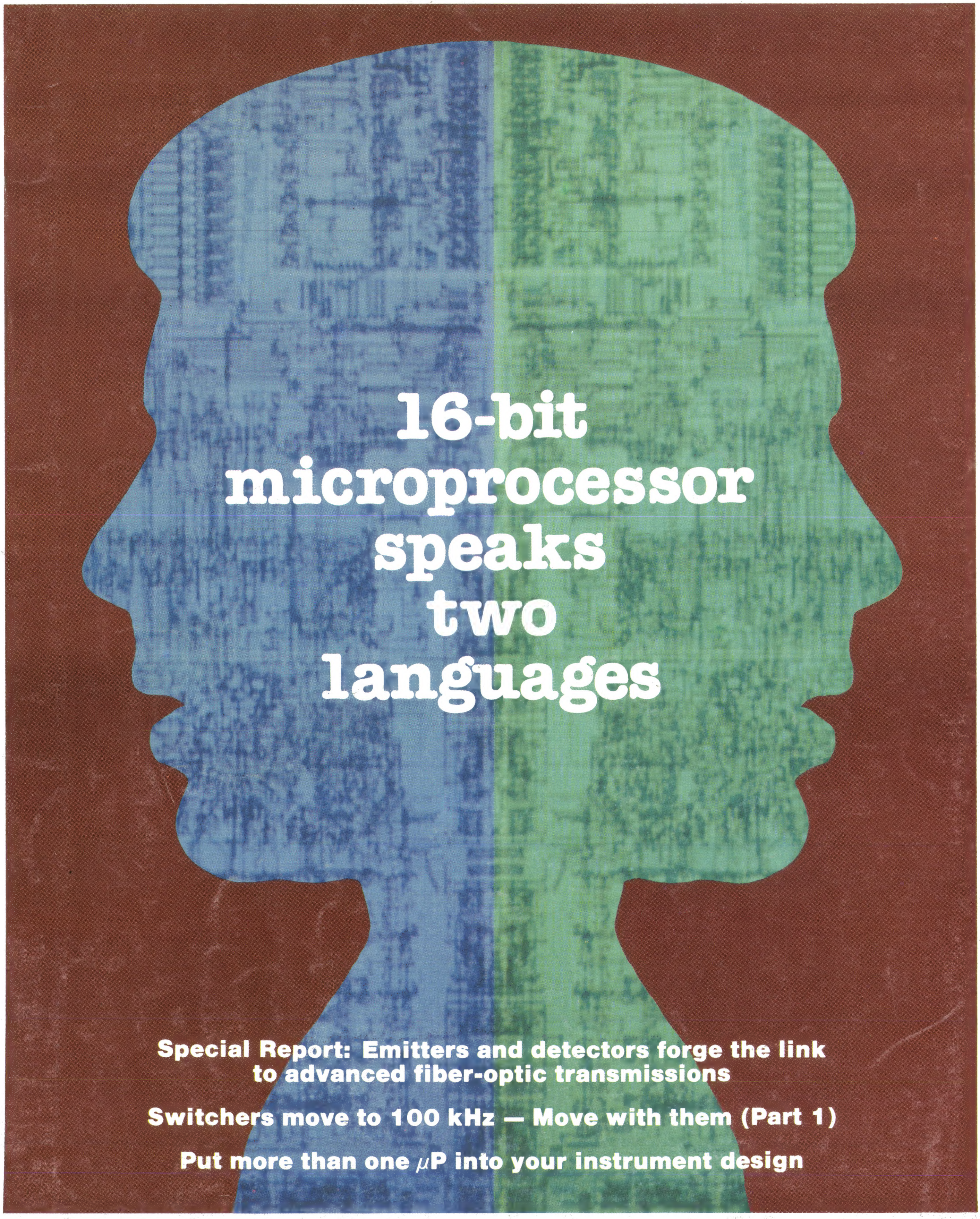
2

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

JAN. 18, 1980



16-bit microprocessor speaks two languages

Special Report: Emitters and detectors forge the link to advanced fiber-optic transmissions

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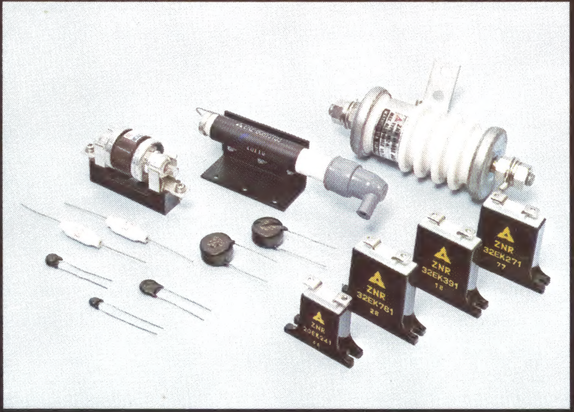

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On the cover: Chip photograph courtesy of National Semiconductor

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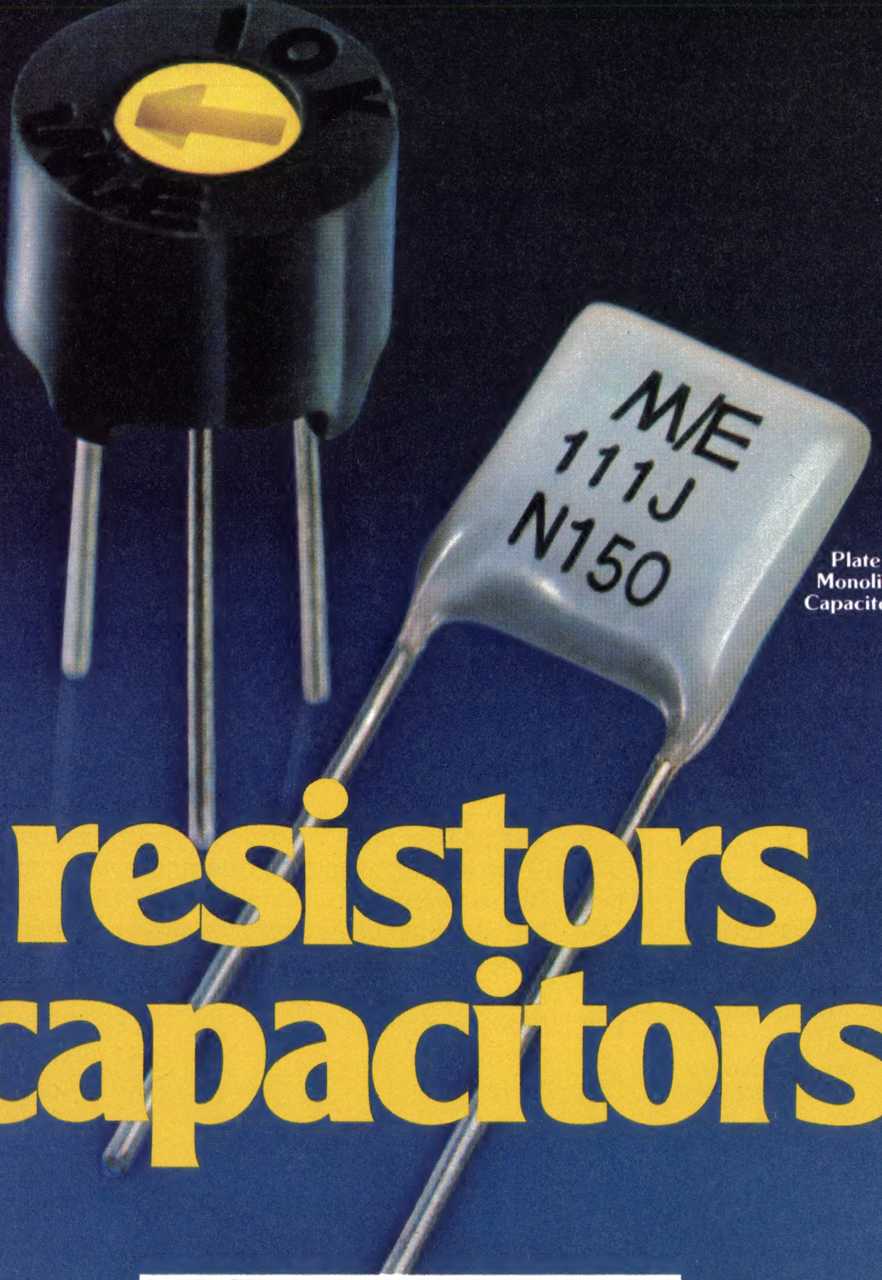

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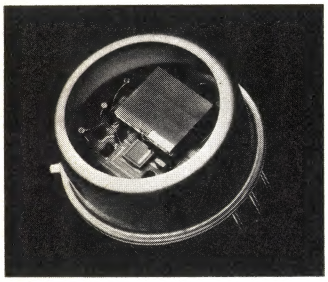
Contents Spotlight



Special Report: Fiber-optic emitters and detectors
Advances abound in fiber-optic emitters and detectors. At wavelengths between 1300 and 1600 nm, optical-fiber loss and dispersion go down. Designers of lasers and light-emitting diodes are creating new schemes to boost emitting power at these longer wavelengths. In addition, detector sensitivity is getting a boost by integrating amplifiers on the same chip as the detector diodes. Indeed, losses are being reduced even further by hermetic sealing, which not only protects LEDs (and some lasers) from temperature variations but also helps direct light efficiently into the fiber. It's time to get a handle on all these developments.

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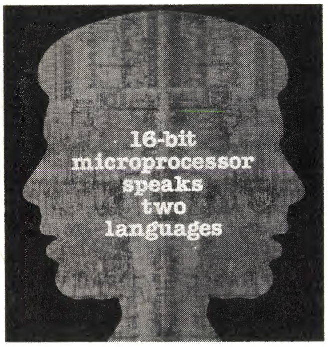

Bilingual 16-bit μP brandishes large-scale computer power
Advanced architecture enables National Semiconductor's NS16000 family of 16-bit CPUs to provide such large-scale computer features as multitasking, memory management to 16 Mbytes, and peripheral control. A symmetrical approach to registers, instruction and data and address modes makes programming the family easy and efficient. All processors have a native set of 100 basic instructions, but the instruction set can be expanded with slave processors and trap mechanisms. In addition, all eight general-purpose registers and several types of data look the same to the instructions.

p. 66

Switcher performance improves at 200 kHz
Increasing the frequency of a switching power supply to as much as 200 kHz shrinks components and thus helps expand performance. But there's more to it than merely raising the frequency. Circuit topologies must be studied to provide the optimum performance. Careful layout and good bypassing must be employed to avoid subharmonic instabilities. Then it all comes together at 200 kHz.

p. 74

Two-chip μC system enlarges memory, not component count
When a one-chip microcomputer system demands more memory or I/O capability than the one chip can supply, instead of adding extra components that raise the chip cost and count, simply add another one-chip μC. The memory and I/O control is readily accessible, while the extra computer power could help the system carry out its tasks. Here's an example of how this can be done with a simple, low-cost instrument that automatically measures the chemical concentration of a liquid solution. The second μC not only adds its own memory and I/O ports but also takes on A/D-conversion control.

p. 82

SLAVE COMPUTING: AN INNOVATIVE ALTERNATIVE TO MULTI-PROCESSING.

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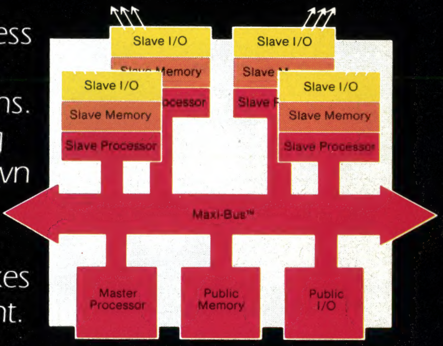

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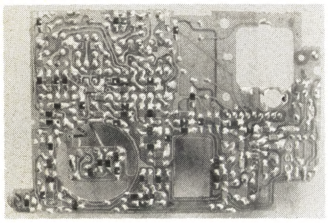

Flow-soldering chip components boost packaging density
A new generation of chip components is bringing dramatic increases in packaging density while reducing production costs. These chip resistors, chip capacitors, chip transistors and chip diodes can be directly flow-soldered on a printed-circuit board along with other components. In addition, they can be attached automatically to either side of a board, or even on both sides. Developed by Japan's Toyo Electronics, the chips may well herald a new era of advances in component density.

p. 90

Construct computer models of pulse-width modulators
Because of their small size and high efficiency, switching power supplies are challenging the traditional dominance of linear supplies. The resultant growth of switchers has spurred the need for modeling pulse-width modulators to evaluate switching-regulator designs. Computer circuit-analysis packages, such as Computer Sciences Corp.'s TRAC and DCD SYSCAP II, make it possible to develop a PWM-inverter model that can be used as a subcircuit. This article shows how to develop the model and use it for analysis of a switching regulator.

p. 94

Intelligent processors transmit asynchronous data errorlessly
Armed with a packet-transmission scheme based on the CCITT X.25 protocol, assemble an intelligent network processor that provides error-protecting envelopes for data being transmitted between network nodes. The processor can place data from up to 30 asynchronous input lines onto a single high-speed synchronous output line. Not only will data be protected but transmission will be transparent and line-use efficiency will go up.

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Electronic Design 3

Featured Next Issue

In the February 1 issue:

Automatic Test Equipment, including a Special Report on board and semiconductor testers...PLUS: Ins and outs of testing codecs and microprocessor and memory boards with signature analysis... Two ways to do signature analysis... Designing 200-kHz switchers (Part 2)... Learn the eight operating modes of a single-chip μC.

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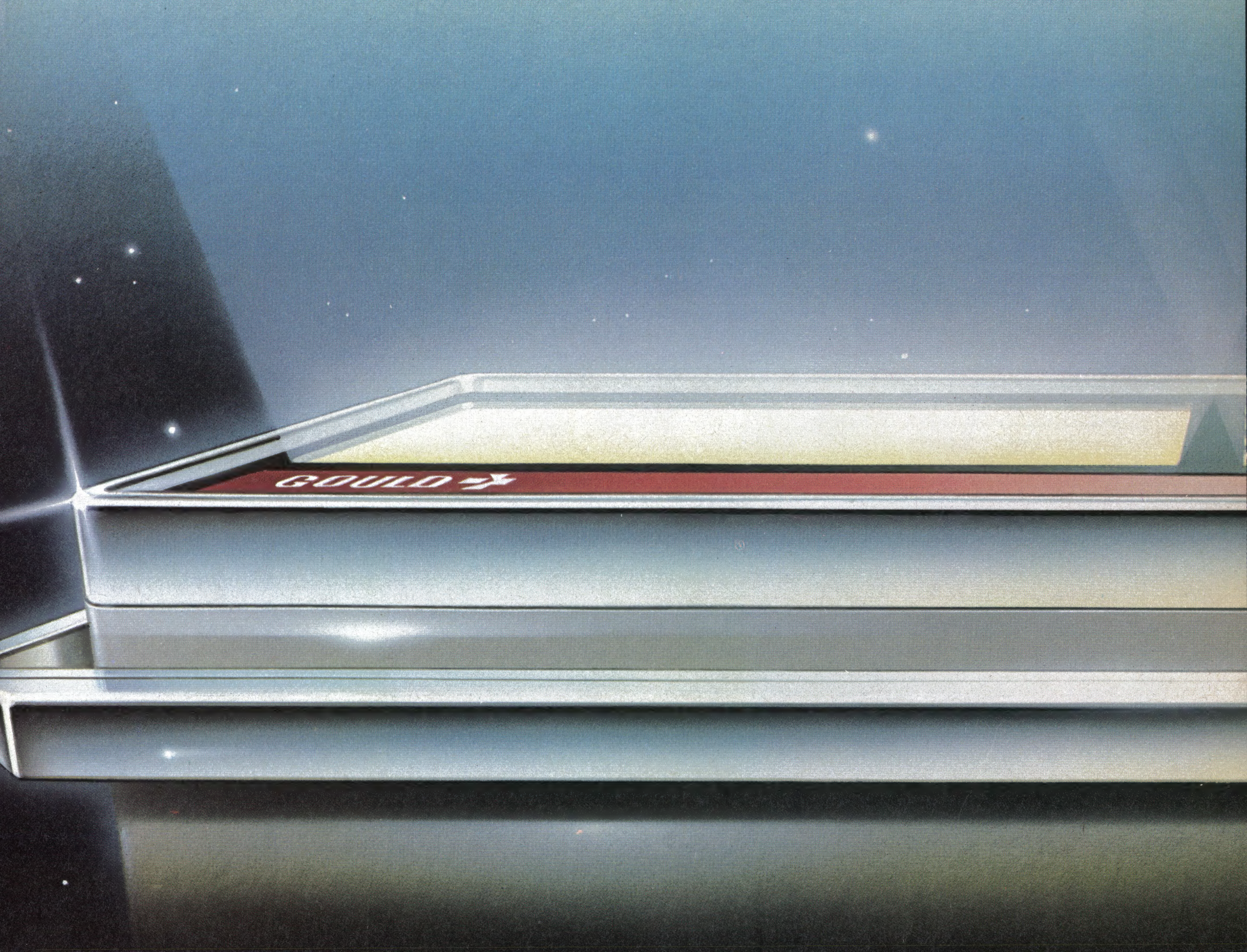

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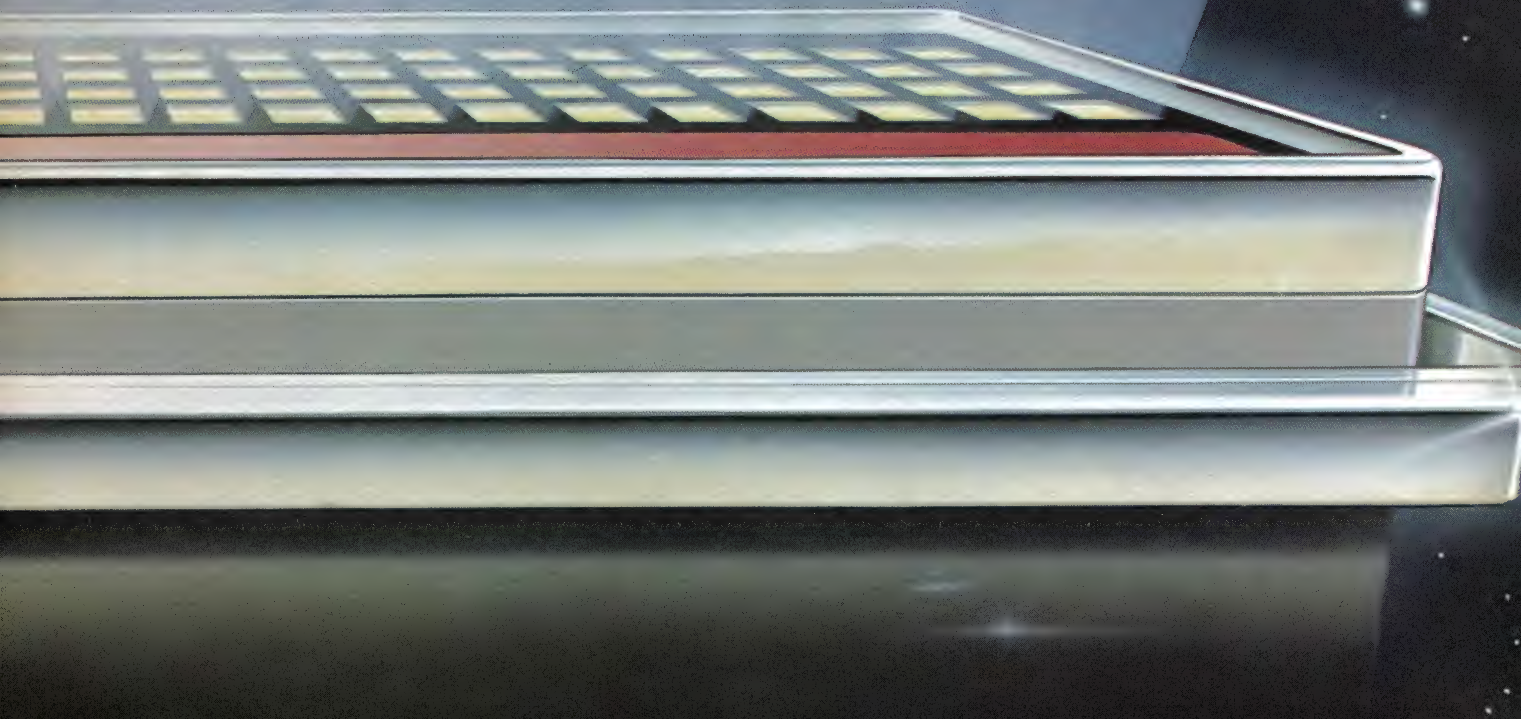

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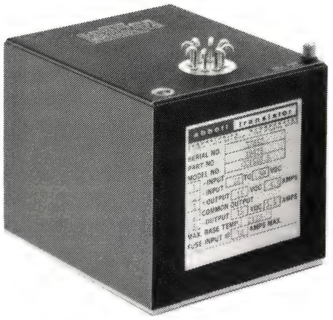

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Reader Feedback

Standards—made to be broken?

It is good to see articles in your journal such as the recent series on Pascal and Fortran; I hope that one on Ada will be next. However, I feel the first of the articles on Fortran 77 (Sept. 13, p. 126) leaves a lot to be desired.

The article claims to be discussing the new standard, with examples from the Intel Fortran-80 implementation. The author, however, does not say that only the subset standard rather than the full standard is discussed, and she mixes the standard and the implementation—for example, in mentioning "bitwise Boolean operations on integers" or in stating that "a carriage return signals the end of a statement." The standard mentions neither of these. The logical IF statement, on the other hand, is shown as new to Fortran 77, even though it appeared in the 1966 standard.

The sample program nicely illustrates the block IF and character features, but omits the end-of-file specifier from the READ statement.

Robert Bell

CSIRO
Division of Atmospheric Physics
P.O. Box 77
Mordialloc,
Vic. 3195 (Station Street, Aspendale),
Australia

The author replies

The series on ANSI-77 Fortran attempted to simplify the material to avoid confusing too many readers. For this reason, the article did not discuss the distinction between the subset and the full standard for Fortran, and occasionally did not clarify the distinction between the standard and the Intel implementation (Fortran-80).

Actually, the Fortran-80 implementation adheres to the subset standard but adds many features from the full standard and others that Intel considers particularly useful for microprocessor applications. Among the former are the logical operators .EQV. and .NEQV., the PRINT statement, BLOCK DATA statements and subprograms. The latter group includes bitwise Boolean operations on integers and the B and Z (binary and hexadecimal) edit descriptors.

The standard does not mention a carriage return to signal the end of a statement; input from punched cards, for instance, does not use this signal. But C/R is a defacto standard for input from terminals.

The sample program was intentionally simplified to highlight certain new 77-Fortran features. It runs correctly under Fortran-80 when input via the default device, here a CRT terminal with keyboard. Other implementations might well call for the addition of an end-of-file specifier in the READ statement.

Christine E. Dickson

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051

Benchmarks benchmarked

Your recent article, "Basic Underlies the Multiple Languages of Smart Instruments" (Oct. 11, p. 94), discusses the increased use of Basic as a programming language for intelligent instruments, and compares a few manufacturers' implementations of the language. In a chart supplied to you by Ithaco you compare the speed of Macbasic with seven other manufacturers' Basic implementations. We have run Bench 1 (performs, 1000 times, the calculation A=K/2*3+4.5) on Macsym 2 and found it took 3.82 s, while the table in your article claims this pro-

(continued on page 14)

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.

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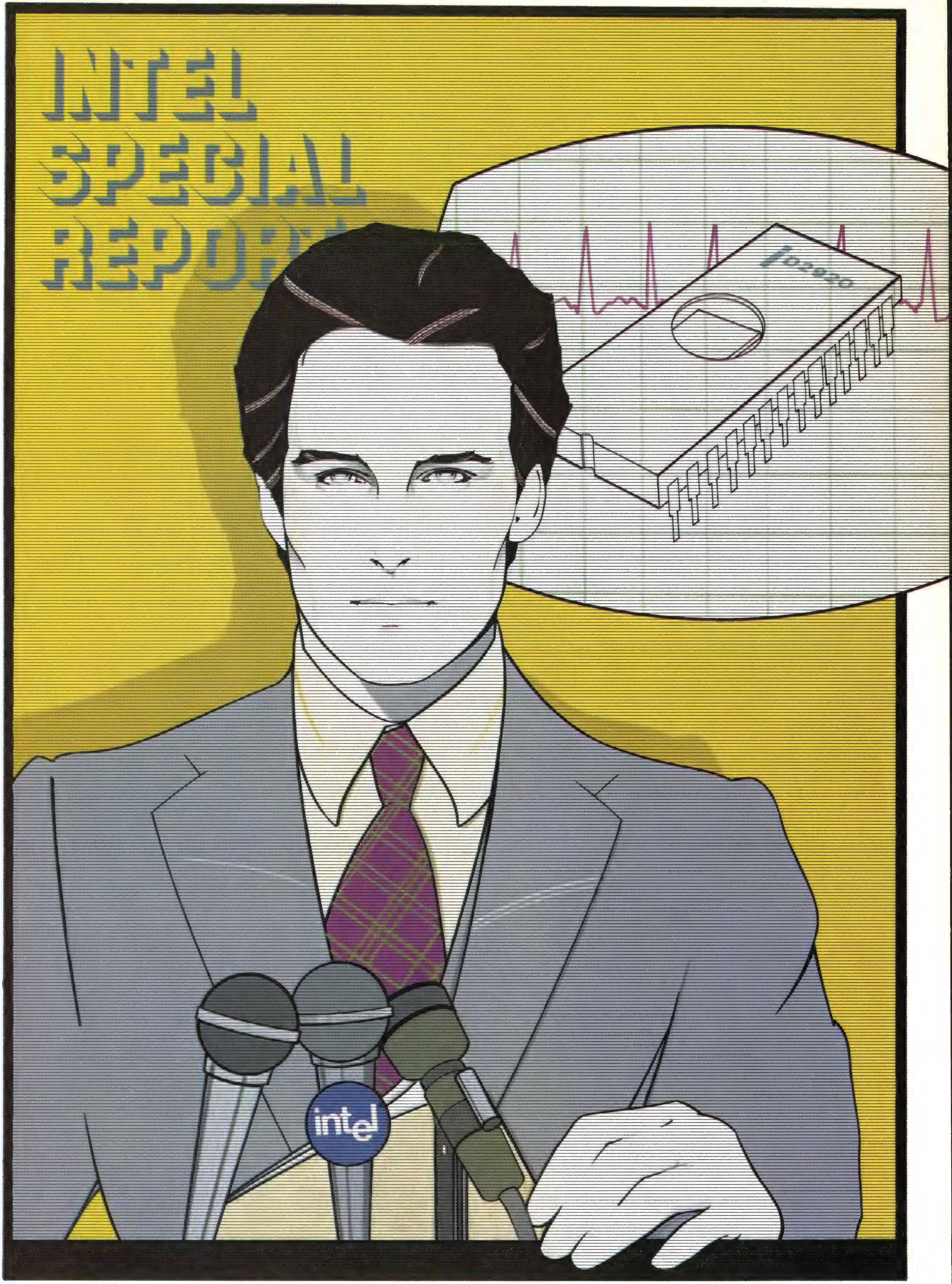
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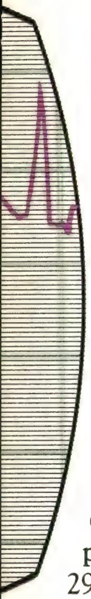
LSI Breakthrough for Analog

Intel announces the 2920 Signal Processor, first general purpose, real-time system on a chip.



Good news for analog designers. Intel breaks a new barrier in microelectronics: The first intelligent chip powerful enough to process analog signals in real time. Plus a computer-aided development package to help speed your systems to market faster than ever before.

Intel's 2920 is a complete, micro-sized signal processing system that packs the equivalent of over 18,000 transistors on a single chip. It operates hundreds of times faster than current digital processors. And best of all, the 2920 allows designers to *program* system values quickly, instead of having to match and tweak components.

A revolution in analog design

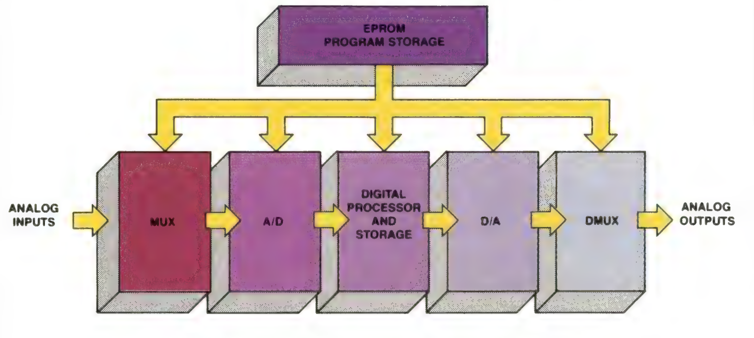
From the beginning, LSI technology has helped designers achieve dramatic improvements in product size, design cycles and manufacturing economics. But until now, the speed and complexity of analog processing has stood in the way of general purpose, single chip solutions for real-time applications.

Today, Intel's 2920 Signal Processor brings the power and flexibility of LSI to the analog world. Because of its size, the 2920 can fit in spaces too compact for traditional analog solutions. Because the 2920 is programmable, product development and time-to-market are speeded significantly. Finally, because the 2920 is a solid state device produced with Intel's proven NMOS process, reliability and manufacturing repeatability are assured to a degree not possible with previous methods.

Micro-processing for the real world

Applications for the 2920 are as broad as your imagination. Since analog designers can program the 2920 processor to perform a large number of standard building block functions, the chip can be used as an entire subsystem. Implement such functions as complex filtering, waveform generation, modulation/demodulation, adaptive processing, and even non-linear functions. This broad capability makes the 2920 an ideal single chip solution for virtually any application in the DC to 10 kHz range.

And like the digital microprocessor, the 2920 is destined to create entirely new classes of applications: products that are smaller, simpler, and less costly to produce. It gives a competitive advantage to companies in such areas as process control, test and instrumentation, guidance or control systems, telecommunications, speech processing, and seismic or sonar signal processing.



Functional Block Diagram of the 2920 Signal Processor

How the 2920 simplifies system development

Programming Intel's 2920 Signal Processor is fast and easy to learn—far less complex than the component matching it replaces. Most importantly, Intel provides the complete support tools and design workshops you need to start designing 2920 systems today.

Our SP20 Support Package and Intel's Intellec® Microcomputer Development System allow you to develop and debug by simulating your system in software. Just program functions according to your system schematic, then specify input and operating values. Together, Intel's development aids let you see how your system will work before you even build a prototype. Best of all, because you develop in digital code, your prototype system will be duplicated precisely in manufacturing.

Start making news with your product

Everything you need to begin designing a new generation of real-time analog processing systems is here today: Intel's 2920 Signal Processor, SP20 Support Package, and the Intellec Development System. For detailed information, including our new 2920 brochure, plus a schedule of Intel's nationwide 2920 Design Workshops and Seminars, contact your local Intel sales office or distributor. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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CIRCLE NUMBER 8

relays

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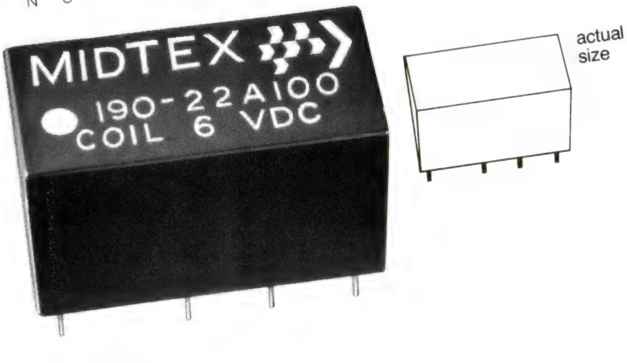

CIRCLE NUMBER 9

Reader Feedback

(continued from page 11)

gram took 15.0 s to execute.

You also state that Macsym 2 does not use the IEEE-488 bus. Please be advised that we do offer a fully compatible IEEE-488 interface as an option on both Macsym 2 and our newly announced Macsym 20.

Edward Soron
Manager of Product Planning,
Measurement and Control Products
Analog Devices
Route 1 Industrial Park
P.O. Box 280
Norwood, MA 02062

Ed. Note: To set the record straight, here is the complete code for Bench 1:

```
300 PRINT "START"
400 K = 0
500 K = K + 1
510 A = K/2 * 3 + 4 - 5
520 GOSUB 820
600 IF K < 1000 THEN 500
700 PRINT "END"
800 END
820 RETURN
```

Ithaco obtained the tabulated value of 15 s on a Macsym 2 without a floating point processor. With one, the execution time was 5.83 s compiled and 6.19 s noncompiled. This is still more than Analog Devices' 3.82 s, but AD's value does not reflect the complete benchmark with its empty subroutine call.

Encouraging response

Congratulations on your recent editorial, "Not for Men Only" (ELECTRONIC DESIGN, Oct. 11, 1979, p. 61). The electronics industry needs this kind of awareness to facilitate the entry of women into the fields of electrical and electronic engineering.

As a "late bloomer" in the electronics circuit design field, I can fully appreciate the statement that women do, indeed, need early exposure to electronics in order to reap all the benefits traditionally available to their male counterparts. Some of this responsibility lies in the hands of secondary education but, as the industry is seeking capable personnel, it should also be actively encouraging the entry of women into a very much male-dominated area.

Candi L. Gunther
Electronic Engineer
E.F. Johnson Company
299 10th Avenue S.W.
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ELEC-TROL BLUE BOY REED RELAYS

NOW TWO GRADES OF LOW-PRICED SEALED RELAYS

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CIRCLE NUMBER 141

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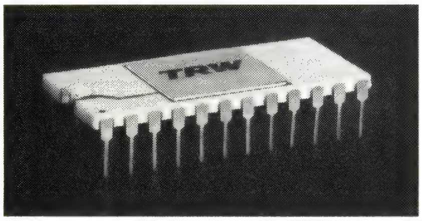

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This new low price will also make it interesting to designers who have been using 4- or 5-bit converters but have longed for higher resolution.

Let us show you how you can go digital . . . economically. Available from stock from Hamilton/Avnet. For immediate information call (213) 535-1831, or send coupon. TRW keeps you ahead in digital signal processing.

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CIRCLE NUMBER 14

INTRODUCING THE BUBBLE MACHINE.

From Fairchild, first family of ATE, comes the solution to the magnetic bubble memory testing problem.

The Xincom 5585 has been developed to test and characterize all currently available magnetic bubble domain memory devices as well as future devices. It's a true general-purpose system that can be used in engineering and production. The 5585 can accommodate various architectures and technologies, and memory sizes up to 65 million bits.

The key to the 5585 is its unique Bubble Memory Pattern Computer (BMPC). This high-speed processor was developed especially for testing bubble memories. It provides the speed and versatility required to execute complex, sophisticated test exercises. We've also developed in the 5585 the most efficient device interface system available – fully programmable current loop drivers, magnetic field coil drivers and precise signal discriminators. So you can exercise your device over an exceptionally wide range of operating conditions.

For engineering characterization, the 5585 is a powerful development tool. For increased throughput, its parallel operation lets you test a number of devices at once – wafers or packages – without compromising test quality. That's an important advantage when you consider the longer test times for bubble memories.

And we haven't forgotten software. No one offers more. A high-level test language, a generalized data reduction library, test management reporting systems, and a highly interactive tester operating system. When you go with a Fairchild test system, you're getting hundreds of man-years of software development. Plus the commitment of the world's leading test system specialist to continue to work with you. As bubble memory technology is developed further, we'll continue to meet your needs – without obsoleting your software investment. This is a big economy when you consider that nearly 75% of your total testing cost is software-related.

The Xincom 5585 is backed by the largest service and support team in the industry. Worldwide training. Over 20 major field service centers in the U.S., Europe and Asia. And a global network of applications specialists to help you get the most from your Fairchild system.

For more information about the Xincom 5585 Magnetic Bubble Memory Test System, just contact your nearest Fairchild sales office today. Or write Test Systems Group, Fairchild Camera and Instrument Corporation, 1725 Technology Drive, San Jose, California 95110. Telephone: (408) 998-0123. TWX: 910-338-0558.

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CIRCLE NUMBER 15

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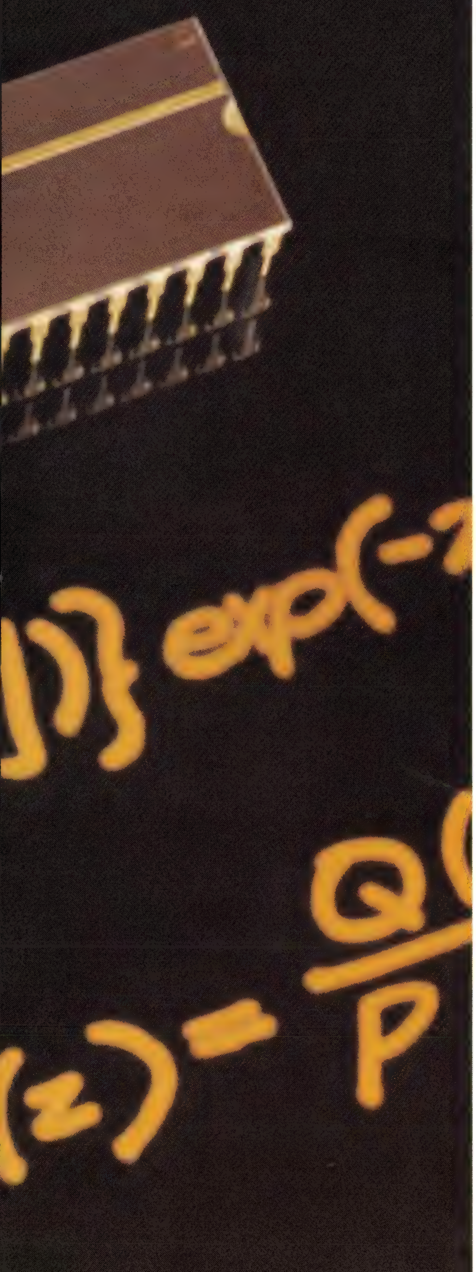

16x16-bit multiplication and 35-bit accumulation in 115nsec

(From a single chip.)

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We have smaller MACs—a 12-bit chip that takes just 95nsec to turn out a 24-bit product and 27-bit sum. And an 8-bit device that produces a 16-bit product and 19-bit sum in a speedy 70nsec.

The power demands of these multiplier/accumulators are downright minimal. Only 1.2W for the smallest, 2.5W for the 12-bit and just 3.5W for the big MAC.

Use them in a high-speed processor and you save hardware, power and bucks... and get better performance in the bargain.

And they're loaded with special features...

- On-chip input and output registers.
- Subtract as well as add in the accumulator.
- Double precision arithmetic.
- Ability to operate as conventional n-by-n bit multipliers.
- Two's complement or unsigned magnitude.
- TTL compatible.
- Operate on +5V.

All this for low prices: in 100's, just $70 for the TDC-1008J 8-bit MAC; $120 for the TDC-1009J 12-bit; and $205 for the 16-bit TDC-1010J.

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TRW keeps you ahead in digital signal processing

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CIRCLE NUMBER 16

Create the right pulse and bring life to your new circuit ideas.

Designing a new circuit is always challenging, but turning an on-paper design into a functioning prototype is where the fun really begins. Signal substitution is an excellent way to speed this process and find potential design faults. For digital applications, the B&K-PRECISION Model 3300 pulse generator is the ideal signal source, because its capabilities are as wide ranging as your applications.

The versatile 3300 lets you independently control pulse period, delay and width. The controls for these functions have seven discrete steps plus continuous vernier adjustment to allow easy selection in the 1Hz to 5MHz frequency range and 100ns to 1 second delay and width ranges. To prevent a control setting that could overlap pulses and create a continuous DC output, an OVERLAP LED signal the operator of an incorrect control setting. Four separate outputs are featured: 600 ohms for general purpose work, 50 ohms for a 15 nanosecond rise time, a convenient TTL output and a trigger output.

For solving family compatibility problems, the 3300 can be used as an interface device to shift pulse levels of two breadboarded circuits of uncommon logic families. Distorted pulse outputs can also be reconstructed so that a clean signal can be fed to a second stage or device. A pulse-burst capability allows the 3300 to also be used as a signal source for testing counters and shift registers. You can even frequency-shift key a function generator, such as the B&K-PRECISION 3010 or 3020.

If your current project is microprocessor based, the 3300 can prove useful as a substitute clock-pulse generator. It's capable of driving several related instruments or circuits independently. One of the most interesting applications for this instrument is to transform an ordinary triggered sweep scope into a delayed-sweep scope. We've designed in a fixed delay mode for quick set-up of scope delay.

The Model 3300 pulse generator is available from stock at your local B&K-PRECISION distributor.

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CIRCLE NUMBER 17
CIRCLE NUMBER 18

Data packets ride coax in Xerox office network

By transmitting data in packets, a passive, coaxial-cable communications network, the Ethernet from Xerox Business Systems, will link various kinds of office equipment within a building without switching logic or central-computer control. Office-system elements like workstations, printers and disk files will be able to communicate with each other; in addition, one system element will be able to send a message to selected groups, according to James S. Campbell, president of the El Segundo, CA company.

Being passive, the network simply accepts transmission packets from attached elements of the system—if one element fails, the others are unaffected. In addition to data, the packets contain addresses of the sending and receiving elements.

Networks consist of one or more segments of coaxial cable, typically several hundred meters long, and one communications transceiver for each communicating element in the system. Each element has a unique address and controls its transceiver. The transceivers, in turn, monitor the network twice:

- Before transmitting, to ensure that it is clear
- During transmission, to detect interference from another system element.

Packets that have been interfered with are retransmitted when the network is clear. Each element responds only to packets carrying its unique address. When reception is completed, the receiving station sends an acknowledging message to the sending station.

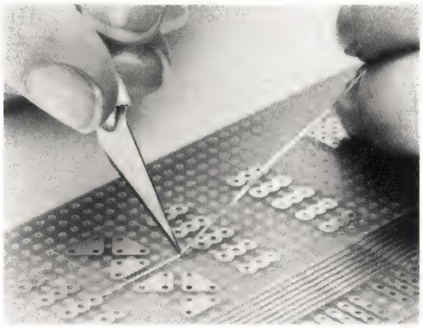
In addition, each Ethernet network has an address that allows internetwork communications. An information packet passing between networks becomes identical to one sent locally and thus is handled the same way within the receiving network. Interconnecting networks or outside access requires additional transceivers and associated processors.

The link is slated for commercial use initially in the Xerox Office Products Div.'s 860 information-processing system. Look for this in the last quarter of 1980.

Color sensor chip frees camera from blooming

A single-chip, high-sensitivity video sensor in a new solid-state color video camera virtually eliminates the blooming that crops up in conventional solid-state cameras. Blooming stems from intense light that causes white vertical streaks to appear in the picture.

While conventional video cameras can suppress blooming only to a level 20 times higher than saturation exposure, the Matsushita camera can suppress it to a level 120 times higher than the saturation exposure, practically freeing the camera from blooming.



The camera, developed by the Matsushita Central Research Laboratories (Osaka, Japan) uses a single photoconductive chip to receive the primary red, blue and green colors. The solid-state image sensor is incorporated with approximately 210,000 picture elements—506 rows, each holding 413 elements. The camera's 280 horizontal and 480 vertical limiting resolution lines offer the highest resolution of any camera in its category. What's more, the highly sensitive camera requires just a standard scene illumination of 500 lux (with an F2 lens).

Conventional sensor panels are plagued with limitations. For one thing, the sensing and transport elements share space on the same substrate—this reduces the area available for sensing and thus sensitivity. As a result, such sensors are not as sensitive as standard image pick-up tubes. In addition, they cannot suppress the overflow of photoelectrons when exposed to the intense light. Blooming results. The Matsushita sensor panel uses a special construction that separates receiving and transporting elements and makes full use of the panel's entire surface for the highest level of light sensitivity. What's more, it enables surplus photoelectrons to be controlled, thereby eliminating blooming, To make all surfaces of the device sensitive to light, the transport area of the panel is laminated with a special low-light photoconductive material called "Newvicon" (also developed by Matsushita).

Coupled with improved overall sensitivity, the reception of the color blue has been enhanced to the point that blue sensitivity is four times that of conventional models. In addition, the transport area employs both a bucket-brigade device for vertical scanning and a charge-coupled device for high-speed horizontal scanning.

The camera is 10 cm high, 6 cm wide and 11.5 cm deep excluding lens. The chip is 13 × 17 mm.

Metal-glass strips strengthen transformers

Ferromagnetic nickel-iron strips formed as "metal-glass" will reduce the size and improve the operating efficiency of transformers, tape heads and other magnetic devices. Called Metglas by Allied Chemical (Morristown, NJ), the metal alloy has unusual tensile strength, approximately one-third the electrical conductivity of steel—and excellent magnetic properties.

Metglas 2826B, for example, has a

permeability on the order of 4400 G/Oe at 10 kHz and 0.002 T induction after annealing. Permeabilities on the order of 700 G/Oe at 500 kHz can also be obtained. In addition, the Metglas compositions are extra hard—85 on the Rockwell scale.

Metglas metals consist of iron and nickel formulations in a "random" atomic structure similar to glass. Rapid quench-cooling, at about 1-million degrees per second obtains the structure. The molten metal is actually frozen before the atoms can form a traditional metallic crystalline structure.

Prototype Metglas transformers developed for 400-Hz aircraft applications easily exhibit one-half to one-third the core loss of a normal transformer—but occupy 82% of the space. Moreover, an experimental 15-kVA transformer developed at MIT's Lincoln Labs, using an average 4.6% of the normal exciting current used by a typical transformer, shows just 56% as much core loss, while running 30 C cooler.

Data acquisition system gets on to Multibus

The latest company to jump aboard the Multibus bandwagon is Burr-Brown (Tucson, AZ). Its Model CS450 stand-alone programmable data acquisition and control system is also the company's first venture into the systems business.

With an architecture based on the 8080 μP and Intel's Multibus structure, the Burr-Brown system can be programmed in Basic-400 and handles up to seven analog and discrete I/O boards in any combination. The boards plug into the Multibus backplane on the motherboard.

In addition to the I/O interfaces, the Multibus provides access to system memory and data transfer between the computer and a pair of minifloppy disk drives that store up to 136 kbytes.

The basic system has 64 kbytes of RAM: 32 kbytes are used by the Basic interpreter and 4 kbytes by the peripherals, leaving 28 kbytes for user programs. The Burr-Brown version of Basic-400 is enhanced with special data-acquisition and control extensions that ease such functions as printer mass-storage controls and multitasking.

Optional hardware includes minicassette transports, 12-in. CRT terminals and a 40-column internal printer.

Briefs

Low-cost, extra-flex-strength fiber-optic cables will soon be available from Brand Rex (Willimantic, CT). A special patented process for stretching and bonding Kevlar reinforcement members increases cable flex strength without increasing the outside diameter. Cable types include single, duplex and triplex fibers of doped and plastic-clad silica with core diameters ranging from 62 to 300 μm. Fiber and cable jackets are PVC.

An intelligent Winchester disk controller provides up to 40 Mbytes of storage for DEC's Q-bus processors. Available from Xylogics, Inc. (Burlington, MA) for $1875, the model 530 controller interface sits on a two-sided, quad-width PC board and employs a bit-slice microprogrammable processor that will help expand system-storage to 960 Mbytes. Availability is 30 to 45 days.

A 19-in. rack systems enclosure will not only allow front loading and vertical mounting of LSI-11 and other DEC Q-bus compatible cards but also expand to accept up to 33 card spaces. Developed by North Atlantic-ACS (Hauppauge, NY), the MCC-1 MicroChassis occupies 7 in. of rack height and is designed so that connections to other enclosures can be made directly from the printed-circuit Q-bus backplane, thereby negating the need for a special interconnect card. A $1195 price tag includes a 100-W power supply with hardware for 12 Q-bus compatible boards.

An analog data subsystem with 16 differential or 32 single-ended analog input channels, as well as two analog output channels, for Nova and Eclipse computers is available from Data General (Westboro, MA). The subsystem, which is supported by the company's RDOS software, features programmable gain on both the a/d and d/a channels. In addition, the $2000 board offers 22-kHz throughput, 12-bit resolution and four voltage ranges.

A PDP-11-based cross assembler that handles 1000 lines of assembly code in half a minute and quickly switches from one target processor to another has been developed by System Kontakt Inc. (Bedford, MA). The MAX-11 consist of 11 software modules directed by a main program. While initial versions handle most popular 8-bit μPs, new versions are coming for the 8086, Z8000, 68000 and LSI-11. Patterned after DEC's VAX-11 macroassembler, the MAX-11 should be easy to learn by VAX users.

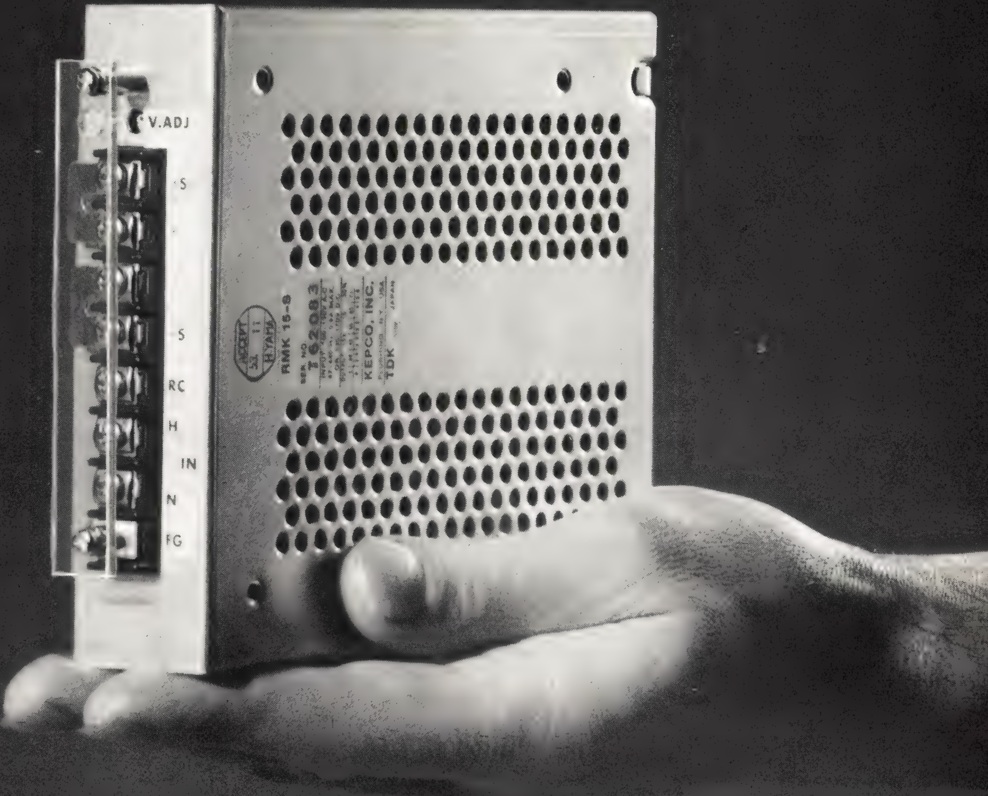
A keyboard based on membrane switches with less than 1-ms bounce fits into rugged, industrial, process-control environments. With a travel of 20 mils, the keys ensure tactile feedback to the operator, and require 6-oz of operating force. Smart versions of the keyboard from TEC, Inc. (Tucson, AZ) will feature on-board scanning, data encoding, mode latching, parity generation, two-key rollover and output strobes.

A μP-controlled test set will ease the testing of frequency-division-multiplexing wire and radio systems. Developed by Hewlett-Packard (Palo Alto, CA), the set consists of a 3586 selective level meter and a 3336 synthesizer/level generator. It makes precise, frequency-selective measurements of such FDM signals as noise, test-tone level, carrier leak and signaling tone; analyzes harmonic level and distortion; and measures intermodulation. Particular SLM models will handle CCITT requirements, Bell specifications, and general-purpose usage.

A pencil-like OCR wand that converts bar code to μP recognizable digital outputs is coming from Hewlett-Packard (Palo Alto, CA). The HEDS-3000, aimed at portable data entry and microperipherals, can read all common barcode formats printed with a minimum bar width of 0.3 mm (0.012 in.) by focusing light from an internal LED emitting at 700 nm and sensing the reflection with an integrated silicon photodetector. Signal conditioning circuitry provides TTL and CMOS-compatible logic level outputs.

think small

KEPCO/TDK switching power modules



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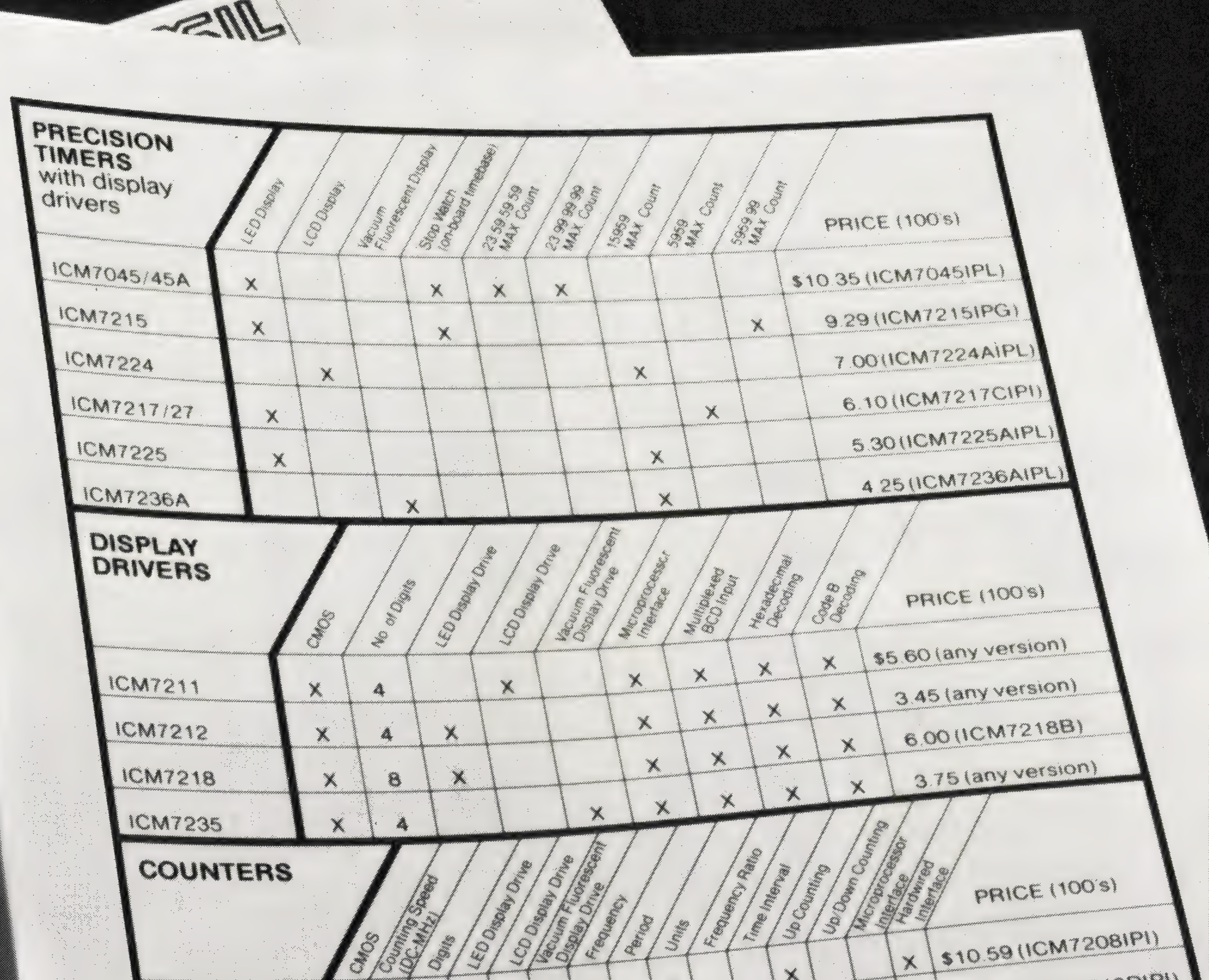
CIRCLE NUMBER 19



PRECISION TIMERS with display drivers	LED Display	LCD Display	Vacuum Fluorescent Display	Stop Watch (on-board timebase)	23:59:59.59 MAX Count	23:99:99.99 MAX Count	15959 MAX Count	5959 MAX Count	5959.99 MAX Count	PRICE (100's)
ICM7045/45A	X			X	X	X				$10.35 (ICM7045IPL)
ICM7215	X			X					X	9.29 (ICM7215IPG)
ICM7224		X					X			7.00 (ICM7224AIPL)
ICM7217/27	X							X		6.10 (ICM7217CIPI)
ICM7225	X						X			5.30 (ICM7225AIPL)
ICM7236A			X				X			4.25 (ICM7236AIPL)

DISPLAY DRIVERS	CMOS	No of Digits	LED Display Drive	LCD Display Drive	Vacuum Fluorescent Display Drive	Microprocessor Interface	Multiplexed BCD Input	Hexadecimal Decoding	Code B Decoding	PRICE (100's)
ICM7211	X	4		X		X	X	X	X	$5.60 (any version)
ICM7212	X	4	X			X	X	X	X	3.45 (any version)
ICM7218	X	8	X			X	X	X	X	6.00 (ICM7218B)
ICM7235	X	4			X	X	X	X	X	3.75 (any version)

COUNTERS	CMOS	Counting Speed (DC-MHz)	Digits	LED Display Drive	LCD Display Drive	Vacuum Fluorescent Display Drive	Frequency	Period	Units	Frequency Ratio	Time Interval	Up Counting	Up/Down Counting	Microprocessor Interface	Hardwired Interface	PRICE (100's)
ICM7208	X	2	7	X					X			X			X	$10.59 (ICM7208IPI)
ICM7216	X	10	8	X			X	X	X	X	X	X			X	13.35 (ICM7216DIPI)
ICM7217	X	5	4	X					X				X	X	X	6.10 (ICM7217CIPI)
ICM7224	X	25	4½		X				X			X			X	7.00 (ICM7224IPL)
ICM7225	X	25	4½	X					X			X			X	5.30 (ICM7225IPL)
ICM7226	X	10	8	X			X	X	X	X	X	X		X	X	16.65 (ICM7226BIPI
ICM7227	X	5	4	X					X				X	X		7.30 (ICM7227AI
ICM7236	X	25	4½			X			X			X			X	4.25 (ICM7236I

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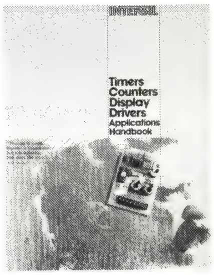

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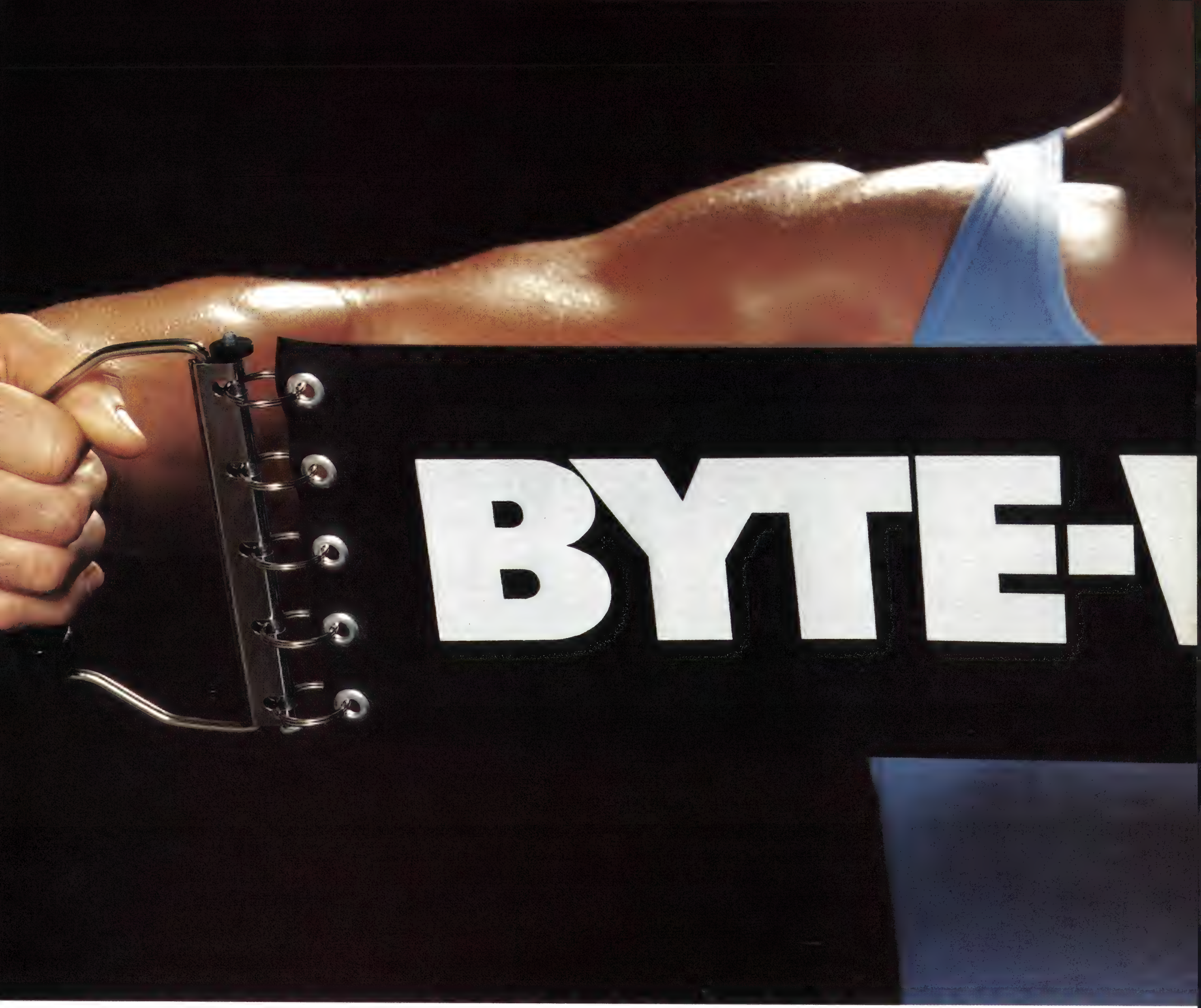

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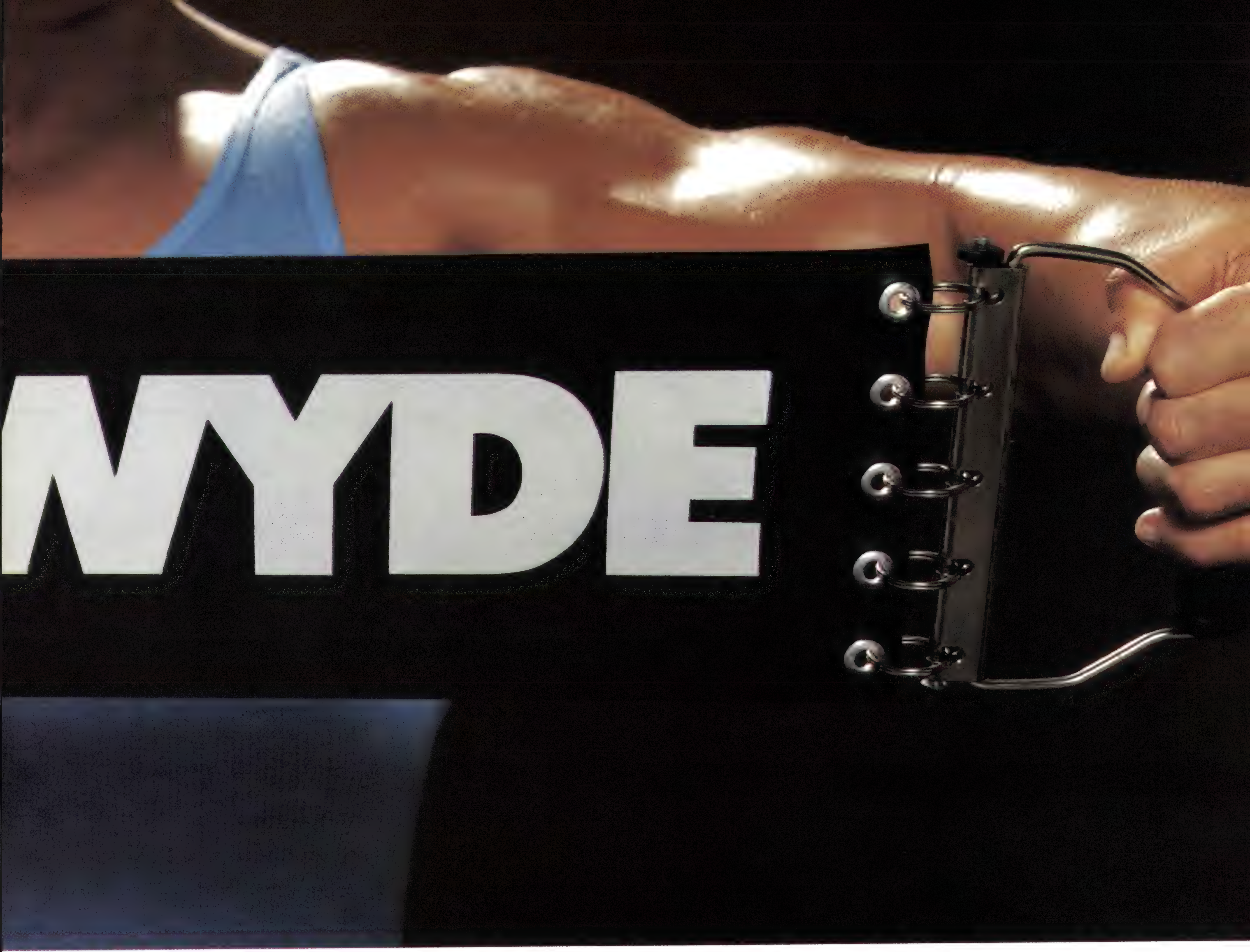

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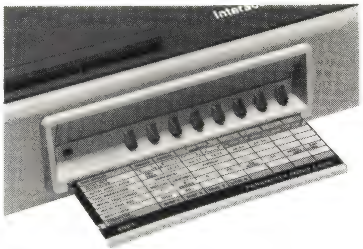

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CIRCLE NUMBER 22

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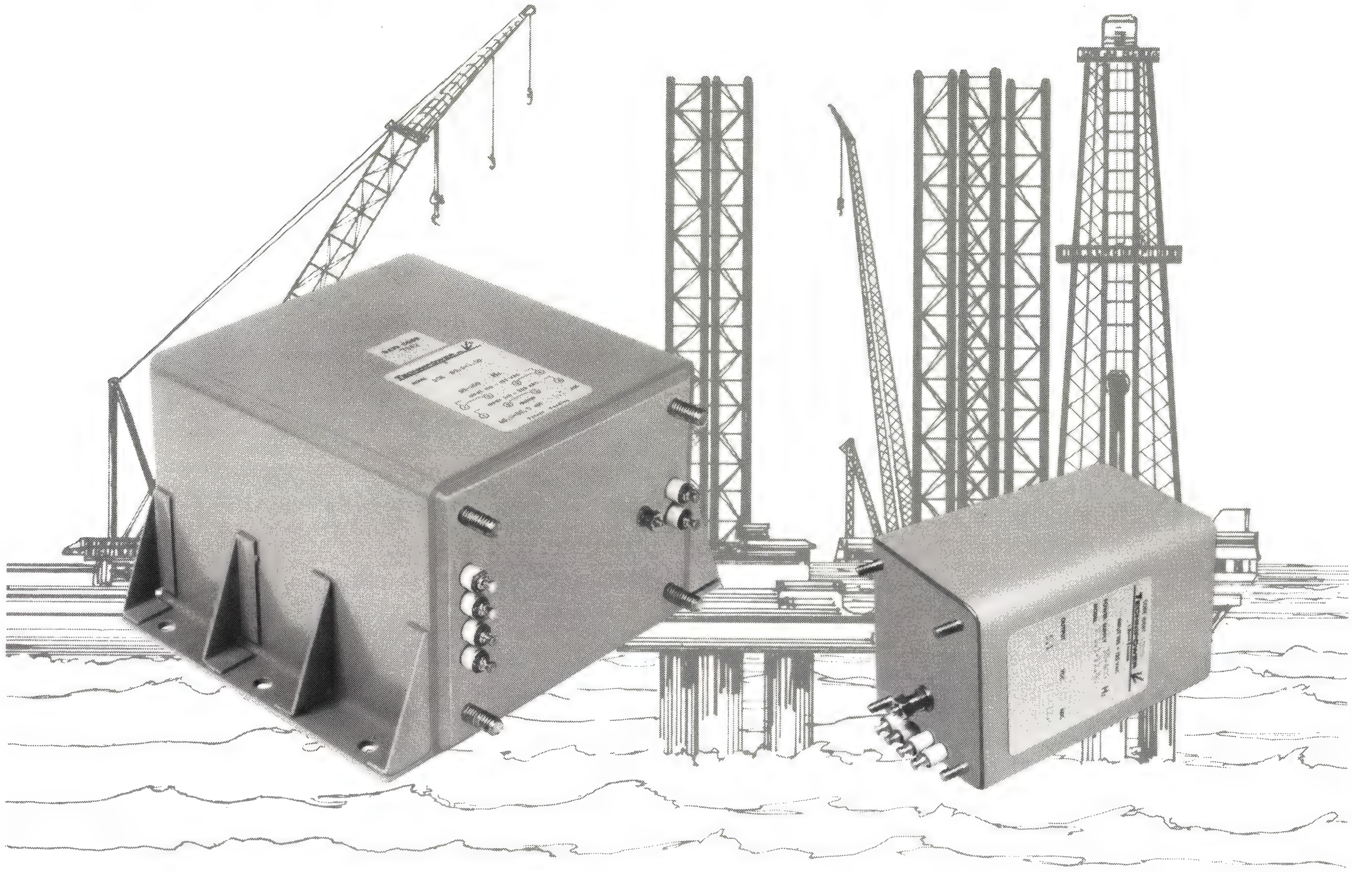

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CIRCLE NUMBER 23

Z8000 CPUs expand processing power with new instructions, special processors

Special-purpose processors and instruction-set expansions will extend the processing capability of Z8000 16-bit CPUs. Releasing previously undisclosed features of Z8000 architecture, Zilog (Cupertino, CA) will use hitherto undefined operation codes along with a series of Extended Processing Units (EPUs) to free the CPU from complex tasks that formerly required considerable CPU time.

Although the EPUs will not be officially announced for several months, the Z8001 and 8002 CPUs that can use them will be shipped after mid-1980.

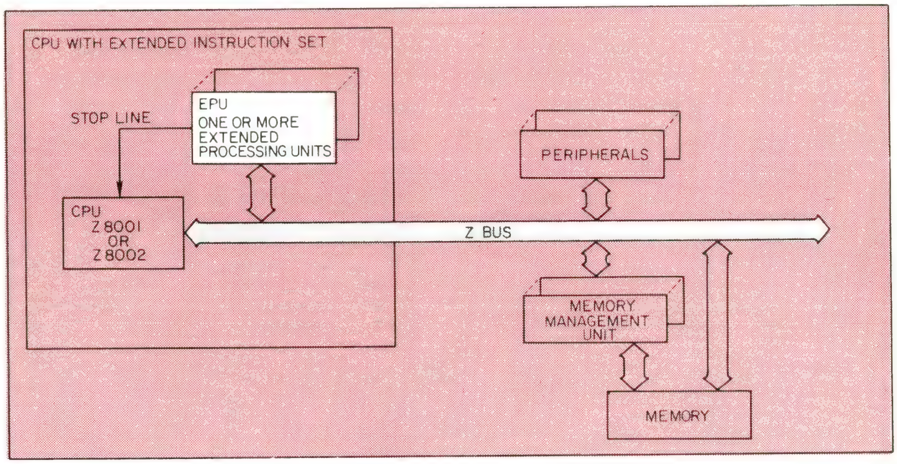
Typical functions suitable for dedication in EPU form include floating-point arithmetic, data-base search and maintenance operations, network interfaces and graphics-support operations. The EPU concept is similar to the concept used by Intel for its soon-to-be announced 8087 math co-processor. The EPU performs its tasks on data resident in its internal registers. The system's Z8000 CPU and software are responsible for moving information into and out of the registers and for telling the EPU which operation to perform.

The enhanced Z8000 instruction set will contain four Extended Instructions: EPU internal operations, data transfers between the memory and EPU, data transfers between the CPU and EPU, and status transfers between the EPU and the CPU status flags. This last command is very handy when the program must branch based on conditions determined by the EPU.

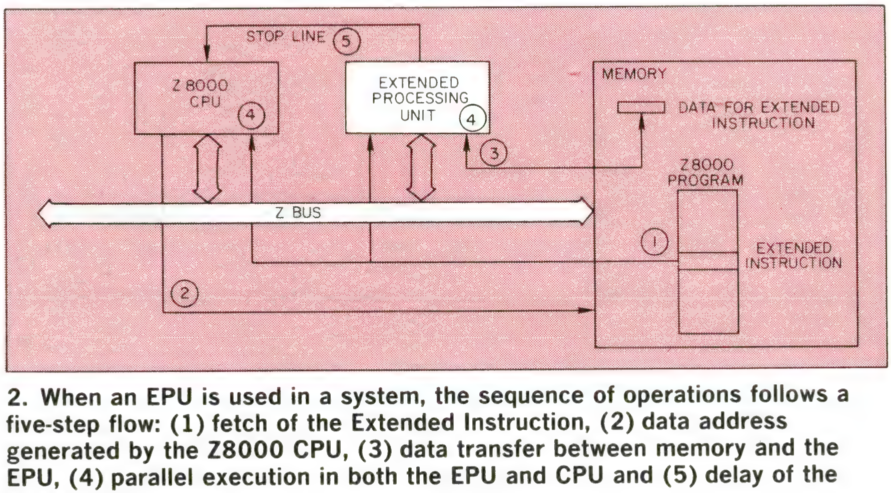
In a system, the EPUs are transparent to most operations and monitor the activity of the CPU's address, data and status lines (Fig. 1). If the instructions fetched by the Z8000 are Extended Instructions, all EPUs in the system and the CPU latch the command (one CPU can control several EPUs). When the instruction must be executed by a specific EPU, as indicated by an ID field in the instruction, then the Z8000 CPU and the selected EPU execute that command.

When the Extended Instruction indicates a transfer of data between an EPU's internal registers and the main system memory, the Z8000 CPU calculates the memory address and generates the appropriate timing signals (for example, address strobe or data strobe). The data transfer itself is between the EPU and the memory—the data do not go through the CPU. The CPU can also transfer data to or receive data from the EPU as if it were a peripheral.

If the Extended Instruction requests that the EPU perform an internal operation, the EPU executes that task, and the Z8000 is free to go on to



1. Adding processing power to a Z8000-based system, the Extended Processing Units mate directly to the Z-bus and monitor the address, data and status lines to determine the desired operation.



2. When an EPU is used in a system, the sequence of operations follows a five-step flow: (1) fetch of the Extended Instruction, (2) data address generated by the Z8000 CPU, (3) data transfer between memory and the EPU, (4) parallel execution in both the EPU and CPU and (5) delay of the Z8000 if Extended Instructions overlap.

Dave Bursky
Semiconductors Editor

its next instruction (Fig. 2). Processing continues simultaneously on both the CPU and EPU until a second Extended Instruction is directed to the same EPU. (If more than one EPU is in a system, all of them can operate simultaneously and independently.) If the EPU is still executing the last Extended Instruction when another request comes along, the EPU temporarily suspends the Z8000's instruction-fetch cycle by activating the CPU's $\overline{\text{STOP}}$ line until the task under execution is completed.

Six Z8000 operation codes are dedicated to the added Extended Instructions. The action taken by the CPU upon encountering any of these instructions depends on a control bit in the CPU's flag and control word register. When this bit is set, it indicates that the system includes EPUs and that the Extended Instructions are executable. If the bit is not set, the CPU performs an instruction TRAP, so that a trap-handler software routine can emulate the desired operation. ■■

Test results help match emitters to fiber-optic cables

Stephan Ohr
Components Editor

An extensive study of the coupling efficiency of fiber-optic emitters and cables suggests that microlens emitters are better for single, small-diameter fibers than domed or pigtailed emitters, and that domed structures are the most effective means of transferring light to fiber bundles. The results of the study, conducted by John Keating, James Levy and David Medved of Meret Inc. (Santa Monica, CA), are shown in the tables.

The cable types explored are listed in Table 1, and include the most popular lines from Siecor, (Horseheads, NY), Belden, (Geneva, IL), ITT Electro-Optical (Roanoke, VA), DuPont, (Wilmington, DE), Canstar (Scarborough, Ontario), Valtec (West Boylston, MA), Maxlight (Phoenix, AZ), Galileo (Sturbridge, MA), Pilkington (Clwyd, North Wales, UK) and QPC (Plainfield, NJ). The fiber types included glass and plastic-clad silica, graded and step-index fibers.

Light sources in the study were limited to LEDs operating in the near-infrared region from 720 to 905-nm wavelength, though the listing included surface emitters, domed and microlens structures as well as LEDs incorporating pigtail structures. While the study could not survey the entire inventory of LEDs, it did survey the most popular devices from manufacturers such as IAV (Van Nuys, CA), Texas Instruments (Dallas, TX), Hitachi (Arlington Heights, IL), Laser Diode Laboratories (New Brunswick, NJ), Spectronics (Richardson, TX) and RCA (Lancaster, PA). The diodes tested are listed in Table 2.

In the tests conducted at Meret, all LEDs were driven in a pulsed mode at drive currents which varied from 5 to 200 mA. Except for the pigtail emitters, each device was mounted in an SMA-type connector which was mated to the appropriately terminated and polished fiber. The fiber was held in place by a coupling nut. The SMA receptacle was also manipulated to obtain maximum signal output through the cable at the receiver end.

Pigtail emitters were coupled to fibers by an SMA-to-SMA, cable-to-cable connector with an estimated loss of −2 to −3 dB, depending on the fiber diameter, and numerical aperture. The output was registered on a fast, large-area detector.

As indicated in Table 3, the combination of surface or domed emitters with multifiber bundles (Type C cable) is entirely satisfactory for low-cost systems with short transmission dis-

Table 1. Typical properties of cables

Parameter	Code designation						
	SC	SD	SE	SG	SH	C	DR
Fiber cladding	Glass	PCS	PCS	PCS	PCS	Glass	Glass
No. of fibers, approx.	1	1	1	1	1	200	19
Index profile	Graded	Step	Step	Step	Step	Step	Step
Core diameter (μm)	50-75	200	250	300	200	62	68
Fiber diameter (μm)	125	600	300	440	400	68	85
Numerical aperture	0.21	0.4	0.35	0.22	0.22	0.66	0.48
Attenuation (dB/km) at: 800 nm	8	60	15	10	10	500	40
900 nm	15	100	30	20	20	500	100
Outer diameter (mm)	4	2.4	5	4	4	2.34	3.81
Minimum bending radius (mm)	50	3.0	40	50	50	6.3	19
Tensile strength (kg)	80	30	80	80	80	2	50
Bandwidth (1-km) (MHz)	200	50	20	20	20	—	—
Bundle diameter (mm)	—	—	—	—	—	1.2	0.43
Weight (g/m)	14	6	13	13.5	13	6	14
Jacket material	PVC	Hytrel	PVC	PVC	PVC	PVC	Kevlar & Teflon

Typical manufacturers:
Type SC: Siecor, Belden, ITT. Type SD: DuPont. Type SE: Canstar, Valtec.
Type SG: QPC, Belden. Type SH: QPC, Maxlight. Type C: Galileo, Valtec.
Type DR: Pilkington, Galileo.

tances (less than 30 meters) and narrow bandwidths (5 MHz).

Microlens emitters, however, put the most amount of power into small-diameter fibers. The ML 37 devices, in fact, seemed capable of putting up to 1 mW into smaller diameter fibers, with much manipulation of the optical elements and the fiber alignment.

Many of the combinations tested were capable of providing significant power levels into the transmission lines at frequencies up to 100 MHz. At "first window" wavelengths, both step and graded-index fibers have losses less than 15 dB per km. With injected power levels at 200 μW and higher, these combinations can deliver more than 5 μW at the receiver after 1 km at frequencies up to 40 MHz. ▪▪

Table 2. IR-LEDs used in fiber-optic data links

Code	ML32	ML33	ML37	M38	ML25P3	ML25P8
Radiated power (mW), typ. @ I_f = 100 mA	1	2	20	2	0.050	0.500
Peak wavelength (nm)	885	905	720	820	830	830
Rise & fall times (ns), typ.	40	12	10	25	1.5	6
Electrical bandwidth (MHz)	8	30	35	15	200	70
Emitter dimensions (mm)	0.5 × 0.5	0.45	0.45	—	0.2	0.075
Emitter type	Surface	Dome	Dome	Micro-lens	Ruggedized pigtail	Ruggedized pigtail
Max. distance from emitter to fiber (μm)	250	250	350	—	10	10
Small-volume unit price ($), approx.	10	20	75-110	100	250	150

Typical suppliers of similar devices:
Type ML32: IAV. Type ML33: TI. Type ML37: Hitachi. Type M38: LDL, Spectronics.
Type ML25P3: RCA. Type ML25P8: RCA.

Table 3. Coupling efficiency of IR-LED into fiber cables

	IR-LED type*					
Fiber type	ML 32 surface emitter (5 MHz)	ML 33 dome emitter (25 MHz)	ML 37 dome emitter (40 MHz)	ML 38 micro-lens (15 MHz)	ML25P3 pigtail (62.5-μm core, 100 MHz)	ML25P8 pigtail (200-μm core, 100 MHz)
C	95	250	1000	750	40	120
SC	3	20	60	70	50	50
SD	25	110	350	300	105	200
SH	20	90	250	300	110	165

*Power levels (μW) injected into the fiber at I_f = 100 mA.

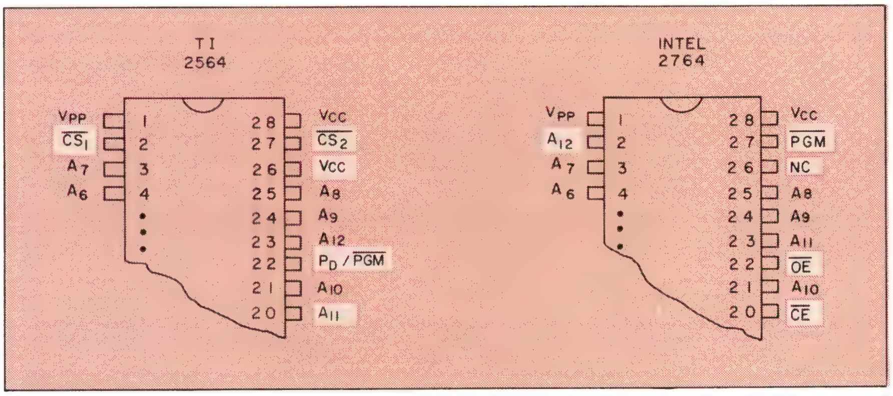
ROM/EPROM/RAM pin compatibility could stretch from 16 to 256 k

With so many different pinouts for identical-capacity byte-wide ROMs, EPROMs, RAMs, and EEPROMs, many new designs have been held back until the confusion of choices clears up. Two 28-pin EPROM layouts—one from Intel, the other from Texas Instruments—should bring designers closer to compatible pinouts for memory capacities ranging from 2 k × 8 all the way up to 32 k × 8.

At the last meeting of JEDEC committee JC42, Intel and TI showed how their respective 28-pin layouts with just a few jumper options could provide the flexibility and growth capability needed to increase memory capacity. Centered on the pinout for the company's 64-kbit UV EPROM, the Intel layout takes into account the various control lines and extra addressing lines that would be required for a totally pin-compatible family of UV EPROMs, EEPROMs, ROMs and static and pseudostatic RAMs.

This concept, approved by the JC42 committee, is the second 28-pin layout to be presented to JEDEC—Texas Instruments (ELECTRONIC DESIGN, Aug. 16, 1979, p. 27) is awaiting final decision. Interestingly, both Intel and TI already have received approval for 24-pin, 32-kbit UV EPROM pinouts. But as densities go beyond the 32-kbit level, the 24-pin package must be upgraded to 28 pins, unless several functions are multiplexed on one pin—as Motorola did for its 64-kbit UV EPROM.

Even a dual standard for 32-kbit and larger memories is far from the ideal, since different PC-board layouts must be developed, depending upon whose memories are used. And if RAMs, ROMs or EEPROMs are to fit in the same socket, which pinout



Although the 28-pin pinouts of the Texas Instruments and Intel 64-k UV EPROMs are identical in function, they differ in control-line placements.

Dave Bursky
Semiconductors Editor

would really provide the optimum flexibility?

For these reasons alone, it is important to note that the Intel pinout differs substantially from the TI one in control-pin assignments. And there are other, more critical differences (see Fig).

The TI 2564 has a dual-function control line on pin 22 that, when high, keeps the memory powered down and, when brought low, activates the memory so it can respond to either of the chip-select signals on pins 2 and 27. In the low state, the line also acts as the programming control.

Intel's 2764 also has a chip-select function, but it's referred to as the Output Enable (OE) and located on pin 22. And for chip power-down, Intel sets aside a Chip Enable (CE) line on pin 20. Clearly, the pins are not compatible by location, even though for read operations the control lines are functionally identical.

The only two control and power lines that are consistent between Intel and TI are pins 1 and 28—the V_{PP} high-voltage programming line and the V_{CC} power-supply line, respectively. Here, though, is where Intel's promises of system compatibility seem to be bear fruit (see Table).

Pin 1 can not only serve as the high-voltage level input during EPROM programming, but can be defined for other functions for other class devices. For example, as EEPROMs become available in the same pinout, pin 1 could serve as the high-level write and erase-control input.

For pseudostatic memories such as an 8-k × 8 RAM, the pin could serve as the external refresh input. However, for RAMs, the line should be implemented as active high, not active low as currently called for. In this case, when pin 1 is tied to V_{CC}, the RAM would be self-refreshing, thus permitting EPROMs or RAMs to be used interchangeably.

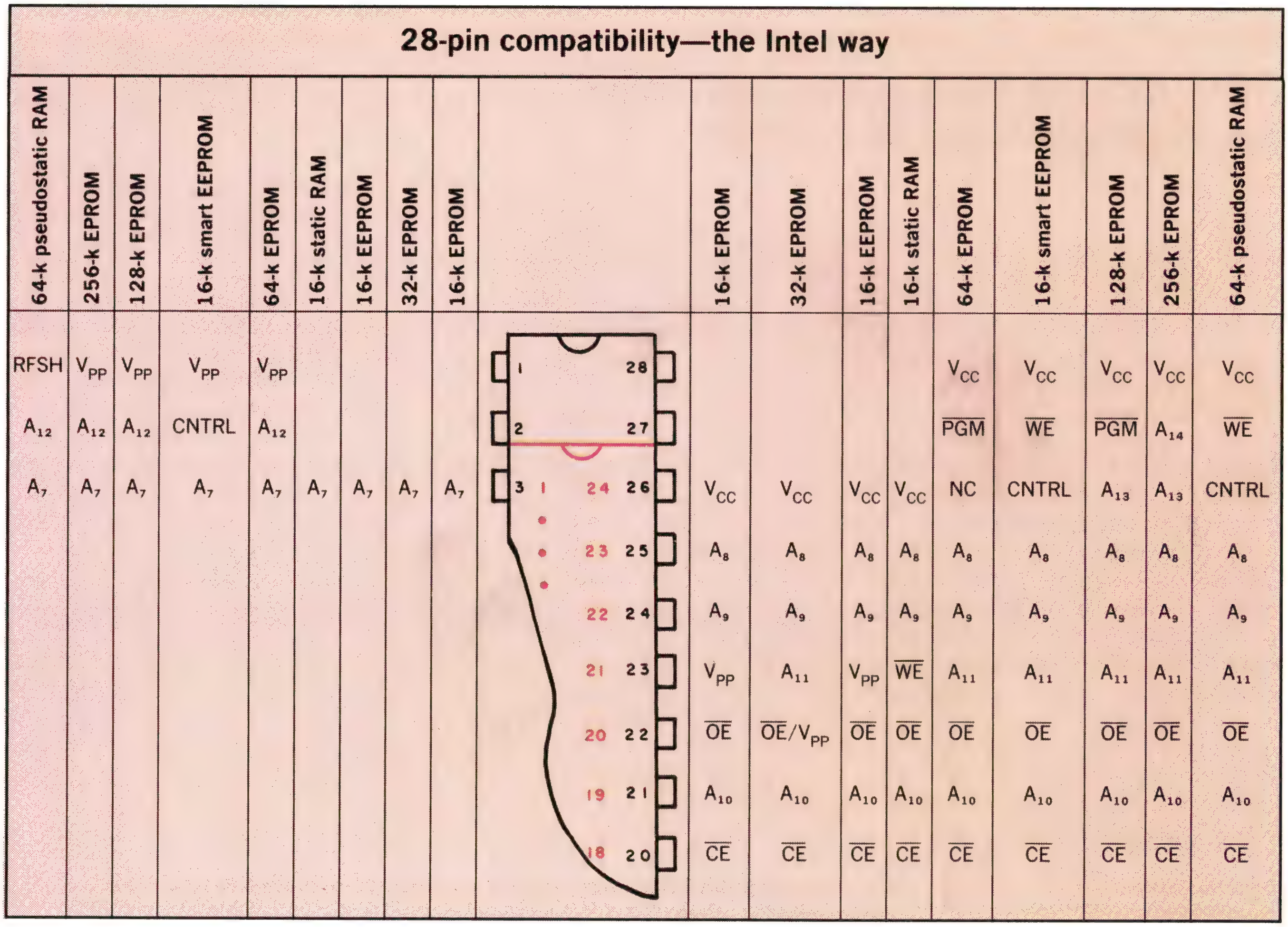
Pin 2 has been set aside by Intel to be the A_{12} address line for 8-k × 8 and larger memory components. Moreover, it will serve as a control connection for "smart" EEPROMs, which contain all the timing and control circuitry necessary to generate write and erase pulses of proper-length. (Regular EEPROMs require external circuits to generate the proper-length pulses.)

On pin 27, the writing function for all compatible units will find a home. For EPROMs, this pin is called PGM, while for both the EEPROMs and pseudostatic RAMs, the pin will carry a Write-Enable label (WE). And when the technology permits a 32-k × 8 EPROM, the pin will become A_{14}.

Pin 26 will serve as a no-connect on the 2764 EPROM. However, for the other memories it will serve as:

- The A_{13} address line for 16-k × 8 EPROMs.
- The CNTRL line for 2-k × 8 EEPROMs
- The CNTRL line for 8-k × 8 pseudostatic RAMs
- The V_{CC} supply for 24-pin memory packages.

The JC42 committee has already approved the initial Intel proposal and is currently trying to amend it with a request from Mostek that the V_{PP} function for UV EPROMs, assigned to pin 1, be allowed to share the OE line, pin 22, as an option to using pin 1. The pinout proposal from Texas Instruments, still awaiting final balloting, should be resolved by the next meeting of the committee, which is slated for February. ■■



28-pin compatibility—the Intel way

64-k pseudostatic RAM	256-k EPROM	128-k EPROM	16-k smart EEPROM	64-k EPROM	16-k static RAM	16-k EEPROM	32-k EPROM	16-k EPROM		16-k EPROM	32-k EPROM	16-k EEPROM	16-k static RAM	64-k EPROM	16-k smart EEPROM	128-k EPROM	256-k EPROM	64-k pseudostatic RAM
RFSH	V_{PP}	V_{PP}	V_{PP}	V_{PP}					1 28					V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
A_{12}	A_{12}	A_{12}	CNTRL	A_{12}					2 27					$\overline{PGM}$	$\overline{WE}$	$\overline{PGM}$	A_{14}	$\overline{WE}$
A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	3 1 24 26	V_{CC}	V_{CC}	V_{CC}	V_{CC}	NC	CNTRL	A_{13}	A_{13}	CNTRL
									23 25	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8
									22 24	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9
									21 23	V_{PP}	A_{11}	V_{PP}	$\overline{WE}$	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
									20 22	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
									19 21	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
									18 20	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$

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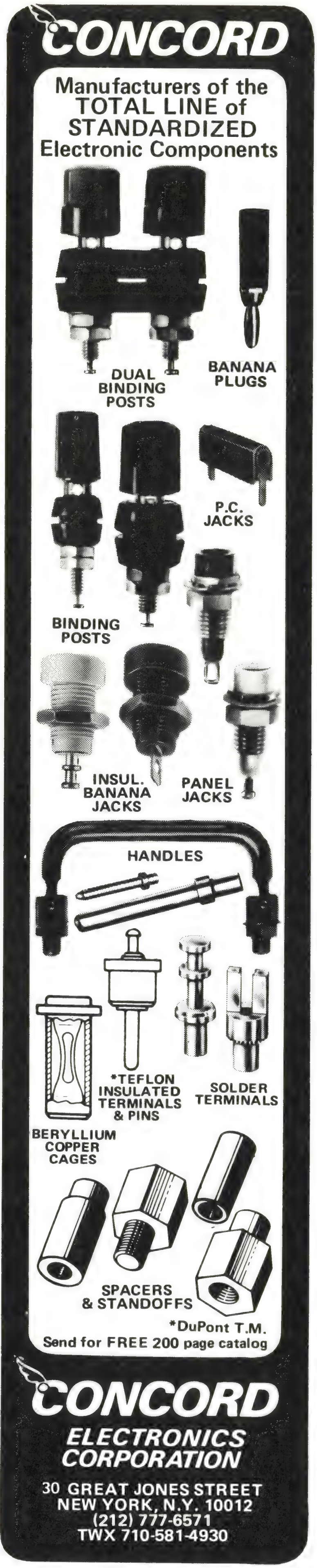
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CIRCLE NUMBER 25

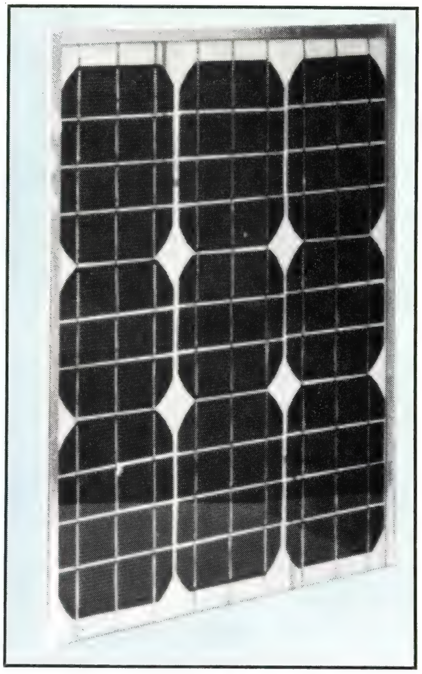
Solar cells move toward larger capacity, lower cost

As concern about the nation's fossil-fuel dependence grows almost daily, the federal government grinds away toward its 1985 goal of creating a self-sustaining photovoltaic industry capable of producing 1000 MW annually. The signs are encouraging. For example, the cost of silicon, while still the main obstacle, has been cut in half in the past two years. A the same time, photovoltaic capacity, while not nearly enough to make a self-sufficient industry, has been doubling every year.

In the financial end, solar-module prices have shrunk from \$22 per peak watt in 1977 to as low as \$6/W_p today. That's still a long way from 70¢/W_p, at which point the capital cost of a solar-voltaic installation, amortized over its lifetime, will be cheaper than fossil-fuel power. At this point, then, the search is on for the technique that turns the solar-cell story around.

One approach to solar-voltaic cost reduction currently under investigation is to pack the containment modules more densely with solar cells, as Motorola (Phoenix, AZ) has recently done. By cutting large-diameter wafers into 4-in. squares, the company has been able to boost active-cell packing density from 69% to 82%, while increasing per-cell efficiency from 10% to over 13%. In the works is a ribbon-growth technology that, according to Marketing Manager Bob Hammond, will replace discrete wafers.

Stacking solution



Array of 4-in. square solar cells from Motorola increases active cell packing density to more than 80%.

Another cost-reducing strategy is a multijunction solar cell with three stacked discrete cells in optical series. It's from Rockwell International (Thousand Oaks, CA). Different semiconductor materials tune each junction's characteristics to specific wavelengths of sunlight. The top junction, for example, has a 2.0-eV bandgap and converts energy at 6000 A and less. The middle junction has a 2.1-eV bandgap and converts energy from 6000 A to 1 μm. The third junction has 0.8-eV bandgap and 1.0 to 1.5-μm energy conversion. The result? Most of the natural sunlight spectrum is covered by the device.

Another wrinkle

Meanwhile, Hughes Aircraft's subsidiary, Spectrolab, Inc. (Sylmar, CA), has begun long-term reliability tests a Sandia Labs on a 10-kW solar generator. It is a hybrid design that uses excess solar energy to heat water, and is well-matched to loads that need both hot water and electrical power, like food processing plants and hospitals.

The generator reflects what Gene Ralph, Spectrolab's vice president of product planning, sees as the direction in which solar-voltaic R&D is moving—beyond the cost of semiconductor material into "balance-of-system" costs: μP controls, mounting hardware, installation and maintenance costs.

Even though the federal government

Richard Hackmeister
Field Bureau Editor

Up the solar-voltaic capacity

Since 1977, the federal government has sponsored a five-fold increase in the amount of solar-voltaic wattage operating in the U.S.—from 100 kW to 500 kW, according to John Maycock, manager of solar-energy systems at the Dept. of Energy. And the department has contracted with various manufacturers to produce almost a full MW in 1980.

The largest installed system in the U.S., the 60-kW facility at Mt. Laguna near San Diego, CA, is scheduled to be surpassed in February by a 100-kW installation at the Natural Bridges National Monument near Monticello, UT. This in turn will be eclipsed by a 250-kW station at the Sky Harbor Airport in Phoenix, AZ.

Meanwhile, the Solar Energy Research Institute of Boulder, CO, an arm of DOE, is working with firms such as Mobil-Tyco, Motorola, Westinghouse and Honeywell to develop less costly materials and manufacturing processes. Just sawing boules of silicon into wafers is almost as costly as producing the material itself, according to SERI director Dr Paul Rappaport, and these firms are working on silicon ribbons.

projects the 1986 cost of solar-cell modules at 70¢/W_p, that does not indicate the ultimate price. "Balance-of-system costs will boost installed residential system prices to between \$1.60 and \$2.20/W_p," indicates Tony Pearson, Manager of Program Administration at the Jet Propulsion Laboratory.

That cost range is the ultimate U.S. goal, according to Pearson, and will result in lower-costing solar power than fossil-fuel power for three main regions of the country: northeast, southwest and southeast—the northeast, because of its higher-than-average energy costs; the latter two regions, because they lie along the nation's sun belt. ■■

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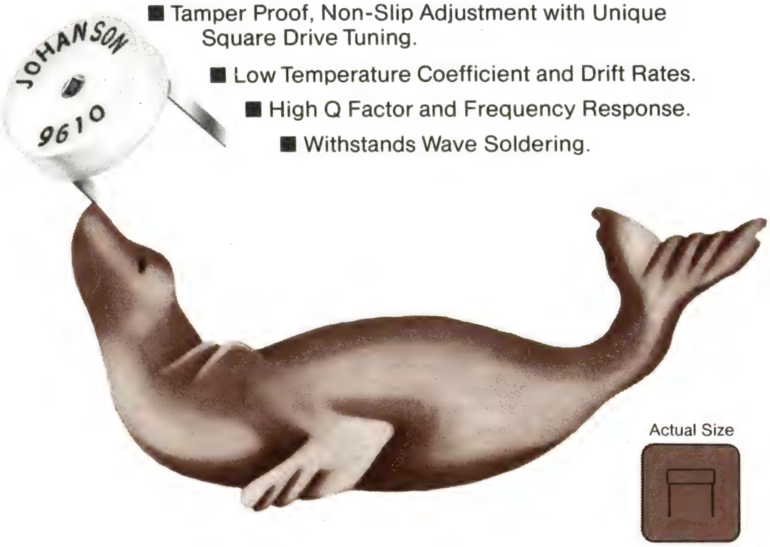

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CIRCLE NUMBER 26

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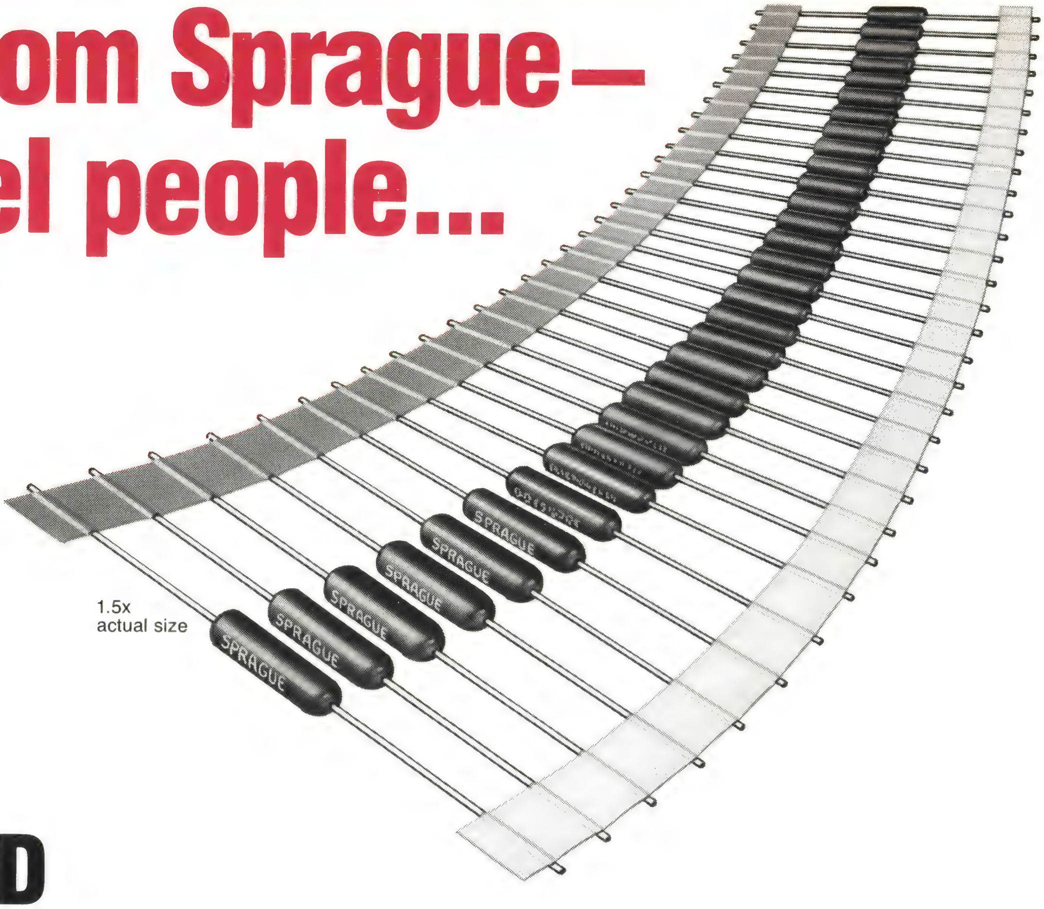

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CIRCLE NUMBER 27

New wrinkles in defense plan: more money, new weapons

President Carter proposes to increase military spending by a real 4.5% per year starting in fiscal 1982, which not only reverses the budget-cutting trend of recent times but also promises to launch what may be the biggest boon to defense contractors since the 1960s.

The plan calls for a $157-billion defense budget for fiscal 1982, with an increase of 4.5% above the prevailing inflation rate in each of the four subsequent years. The fiscal-1980 defense-spending level is expected to reach $127.4-billion, the fiscal 1981 level $142-billion.

Much of the increased funding will go toward already-announced projects like the MX missile, Navy modernization and a new fleet of cargo ships and planes, say administration officials. However, a significant share will be aimed at developing sophisticated new weaponry through support of research and development projects inside and outside the armed services.

The plan represents a turnabout in Carter's defense policy. The President said the switch was made to counter Soviet military advances and prepare the country for the "turbulence and upheaval" of the 1980s.

FCC mobile-phone rules may change

Prompted by the success of American Telephone and Telegraph experiments with a new low-power mobile telephone system in Chicago, the FCC has proposed changes in its rules to allow wider use of the new system.

AT&T developed the Chicago system to handle dramatic increases in the demand for mobile communications, which had crowded the frequencies available in the city. Instead of a single high-power relay station, the system uses many low-power transmitters and receivers stationed in "cells," which are connected to cover the entire city. The mobile phones automatically switch to the frequency of the nearest cell as the driver moves around.

At present, the FCC is considering whether to grant AT&T exclusive rights to the mobile system or to mandate "free entry" into the field for other companies working on multicell systems. AT&T has suggested that two systems be set up in each area, with subscribers to one system reaching the other by regular telephone systems.

An FCC final ruling is expected by June, which would enable the first system outside Chicago to become available by 1982, according to AT&T.

U.S. AM spacing scheme gets government go-ahead

The U.S. delegation to a regional radio conference to be held next March in Buenos Aires, Argentina, has been given the go-ahead to seek 10-kHz to 9-kHz reduction in the spacing between AM radio channels—a move that the U.S. hopes will create many new slots on the AM band for commercial broadcasting. The spacing scheme has been approved by the FCC and endorsed by the Commerce Dept.'s National Telecommunications and Information Administration division.

Although the government sees 9-kHz spacing as a way to create new opportunities in broadcasting, the proposal has run into opposition from several quarters. Other nations in the Western Hemisphere, which would have to agree to the reduction, have voiced concern over potential interference. U.S. broadcasters say they're concerned not only with technical problems but with the economic consequences of many new entries in their field.

If the Buenos Aires conference goes along with the U.S. proposal, a meeting will be set up later to apportion the newly created frequencies among the participating nations. Because of that, U.S. officials are cautious about predicting how much spectrum space will be opened up through the switch.

Solar-electric spacecraft engines to drive comet probes

The National Aeronautics and Space Administration has contracted with Boeing Aerospace Co. (Seattle, WA) and Lockheed Missiles and Space Co. (Sunnyvale, CA) for solar-generated electric engines, which will be used with a pair of probes designed to investigate comets, including Haley's comet.

The new engines, the first spacecraft-propulsion system developed for NASA since the 1960s, will use electricity generated by solar panels and electrically charged mercury atoms to generate less than a pound of thrust. In gravity-free space, this will be enough to drive the space probes, NASA scientists say.

After conventional launch, the system could also be used for a variety of earth-orbit and interplanetary spacecraft.

Remote sensing satellites turn civil

To pave the way for private use of the remote sensing satellites now in orbit and planned for the future, the White House has turned over responsibility for the nonmilitary spacecraft to the National Oceanic and Atmospheric Administration, a unit of the Commerce Department. The NOAA will assume control next year.

Eventually, the administration hopes to transfer the civilian satellites to the private sector, perhaps through a quasigovernmental organization similar to COMSAT, which is now an independent company. Other ideas include plans to lease or sell terminal equipment that would enable private users to receive data directly from space.

Currently, the satellites relay earth photographs and information to ground stations around the country. More satellites are scheduled to reach orbit by the mid-1980s.

TI wins stand-alone-modulator court battle

Texas Instruments' struggle to continue marketing its stand-alone rf modulator appears to have been resolved. The District of Columbia Court of Appeals has upheld a ruling by the Federal Communications Commission that allows Texas Instruments to sell the device while the commission reexamines its guidelines for electronic-television accessories.

The waiver was challenged by Atari Corp., a TI competitor, which argued that the FCC should have made TI stick to the present rules until changes became final. Current regulations prohibit the marketing of stand-alone modulators.

The TI modulator enables the company's home computers to interface with regular television sets and provide a video display.

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CIRCLE NUMBER 28

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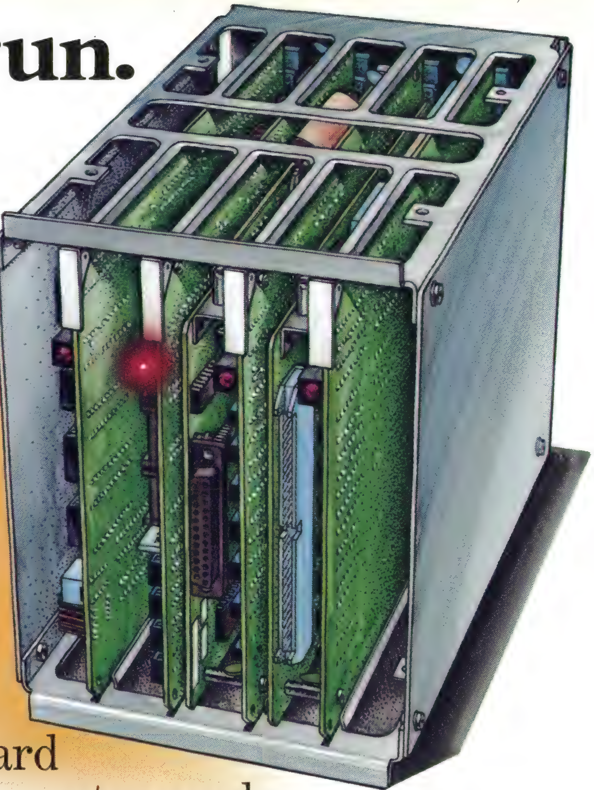

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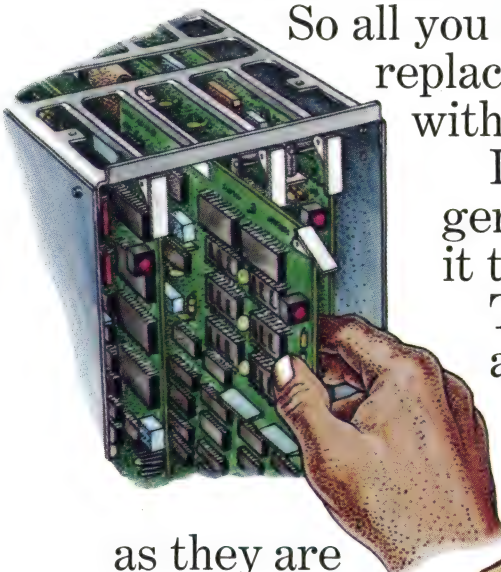

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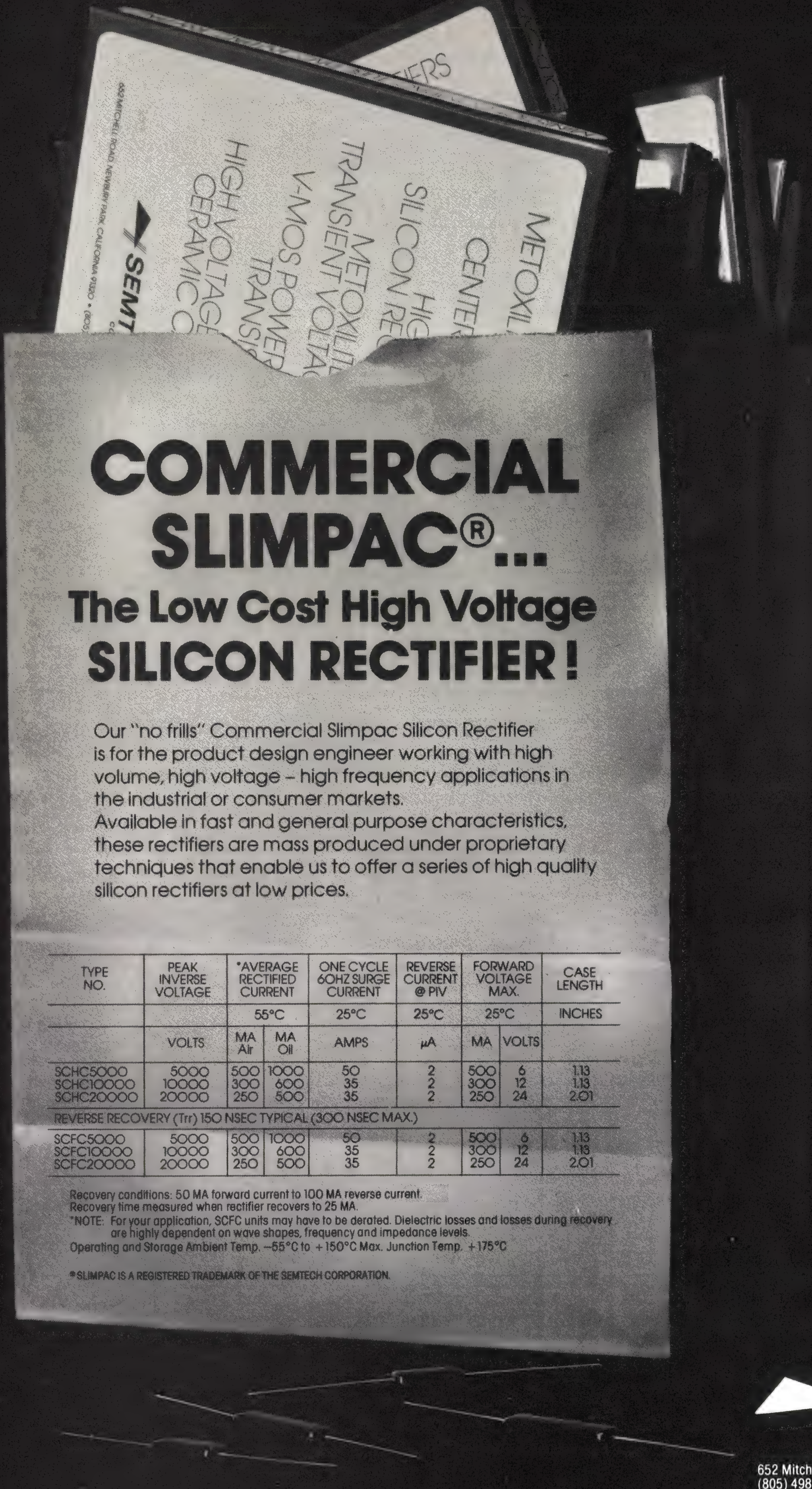
Let's fight for our point at the next design meeting.
Let's make EMI and safety as important as speed or accuracy.
Let's not leave the worry about power or packaging for last.
Let's cultivate planning and avoid expediency.

Let's make productivity a design goal.
Let's innovate, innovate, innovate.
Let's design-in energy savers next time around.
Let's design for the user.
Let's design products to sell, not sell whatever products we design.
Let's keep the public high on technology.

Let's learn the business end of the business.
Let's write more articles for publication.
Let's get active in professional activities.
Let's make engineers as important as other professionals.
Let's keep opportunity in mind and gloom in the garbage can.
Let's refuse to compromise engineering integrity.
Let's have a great year.

Stan Runyon

STAN RUNYON
Executive Editor



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SCHC5000	5000	500	1000	50	2	500	6	1.13
SCHC10000	10000	300	600	35	2	300	12	1.13
SCHC20000	20000	250	500	35	2	250	24	2.01
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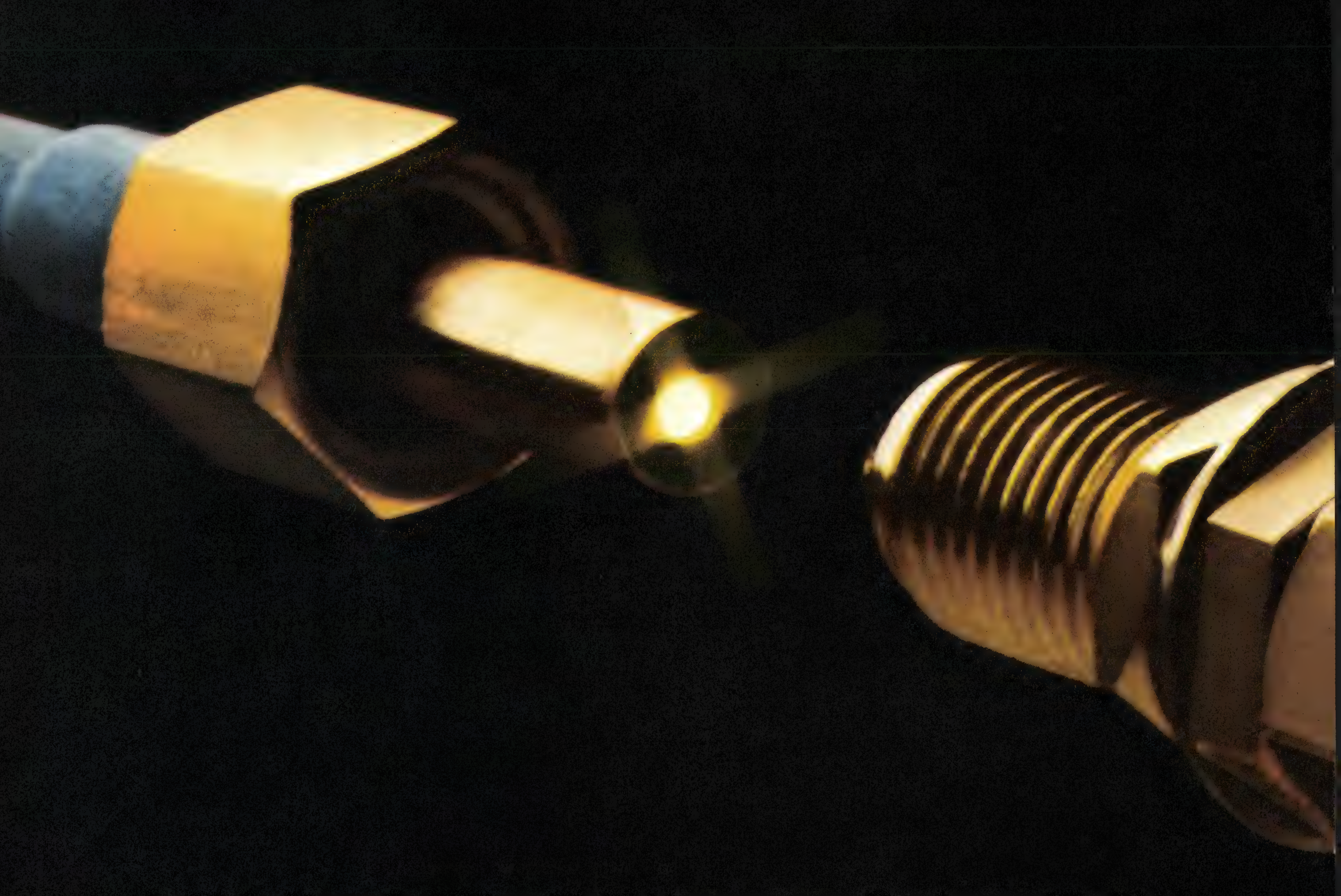
CIRCLE NUMBER 31

GENERAL INSTRUMENT



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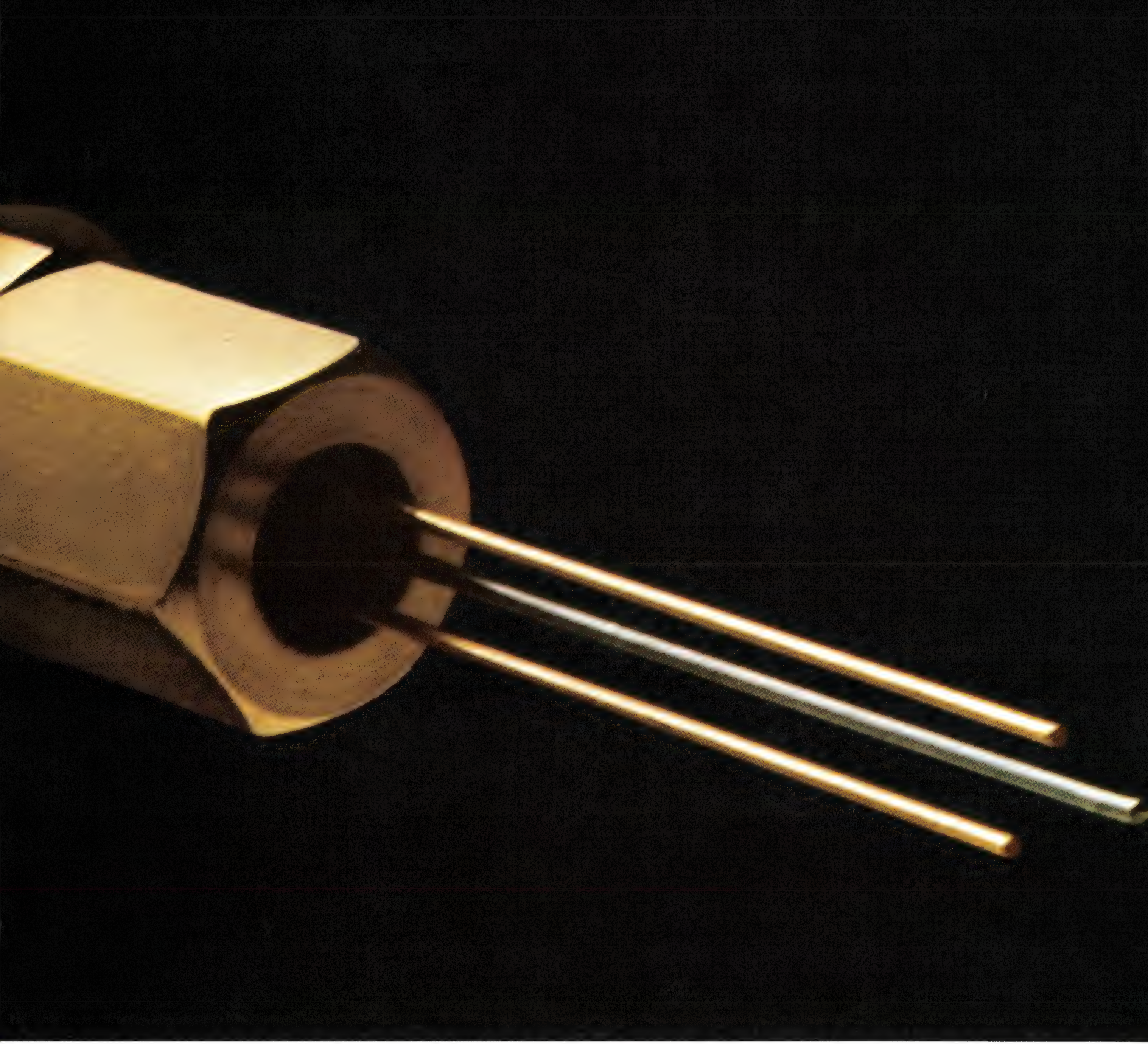

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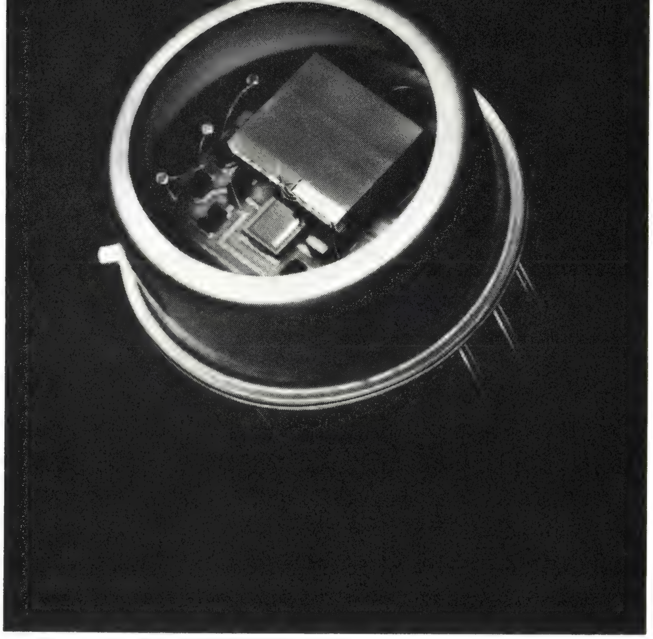
CIRCLE NUMBER 32

Fiber-optic semis carve out wider infrared territory

Stephan Ohr, Components Editor



Light sources and detectors employing advanced heterostructures are opening the way to a second generation of fiber-optic systems having lower cable losses and dispersion. This direction is apparent in the most recent developments in emitters and detectors:

- Lasers now operate at wavelengths of 1300 nm with high power output and long operating life.
- Low-cost LEDs, well regarded for their ruggedness and immunity to temperature variations, are giving longer life and better reliability than lasers at shorter wavelengths.
- GaAs field-effect transistors are replacing silicon p-i-n photodiodes to extend the wavelengths of fiber-optic detectors.
- Single-chip sensor-amplifiers are increasing the effective sensitivity of silicon-diode detectors operating in the shorter wavelengths.
- Hermetic sealing, plastic packaging and other protective measures are improving the reliability and operating life of detectors and emitters.

The so-called "first generation" of fiber systems operated in the visible and near-infrared region of 800 to 900-nm wavelengths. Here, cable losses of 6 dB/km were not unusual and inevitably required the use of repeaters at selected intervals for longer cable runs.

With the latest, "second generation" cable systems, both light sources and detectors function in the far-infrared wavelengths between 1300 and 1600 nm. Fiber losses can approach 0.2 dB/km, and the source's spectral bandwidth is frequently within 10 nm (which encourages the use of single-mode fibers).

A transmitting system that operates between 1100 and 1300 nm has ten times more data capacity than systems operating in the 860-nm region. Such long-wavelength transmission are one benefit of a new generation of injection lasers.

Among the systems that employ long wavelength lasers is an experimental design from Japan's Nippon Telephone and Telegraph (ELECTRONIC DESIGN, July 19, 1979, pg. 33). Tested at 1300 nm, with a 10^{-9} bit-error-rate for 100 Mbits/s, 1.2 Gbits/s and 1.6 Gbits/s, the system proved successful for up to 30 km of fiber, with losses of 0.2 dB/km. A continuous-wave (CW) laser, like that used in the Nippon Tel & Tel System, will provide power outputs of 5 or 6 mW, a forward voltage of 1.5 or 1.8 V and a threshold current of 200 to 250 mA.

Straight shooters

With a rise time of less than 1 ns (250 ps typical), injection lasers are also equipped to operate in the GHz range. Since the far-field beam divergence (the elliptical pattern the light makes at it emerges from the laser) is within 10 x 35 degrees, the lasers are "straight shooters." Cable-fiber attenuation is less than 0.2 dB/km as the light shoots through the fiber.

Several devices—the Series 123 injection laser diode from Laser Diode Laboratories (New Brunswick, NJ), the C86013E edge-emitting diode from RCA (Lancaster, PA) and a unit under development at Hewlett-Packard (Palo Alto, CA)—will employ layers of indium-gallium-arsenide-phosphide (InGaAsP). LDL's 123 series laser has four semiconductor layers: A quaternary, p-type, 2-μm InGaAsP layer is sandwiched between two binary InP layers, covered by an n-type InGaAsP layer. This covering makes a reverse-bias blocking diode and confines the current to the narrow area of the lasing stripe. The RCA unit has a similar structure, but is terminated with a pigtail of Siecor, 62.5-μm diameter, graded-index fiber and a Siecor T-11 connector.

A long-wavelength laser from Bell Laboratories (Murray Hill, NJ) will operate at a wavelength of 1550 nm and provide almost zero dispersion into a very thin single-mode fiber with a 62.5 μm core (and a 125-μm OD). Later this year, Hewlett-Packard will be announcing its long-wavelength light source, employing the InGaAsP technology that will extend the range of its popular data links.

Threshold currents drop way down

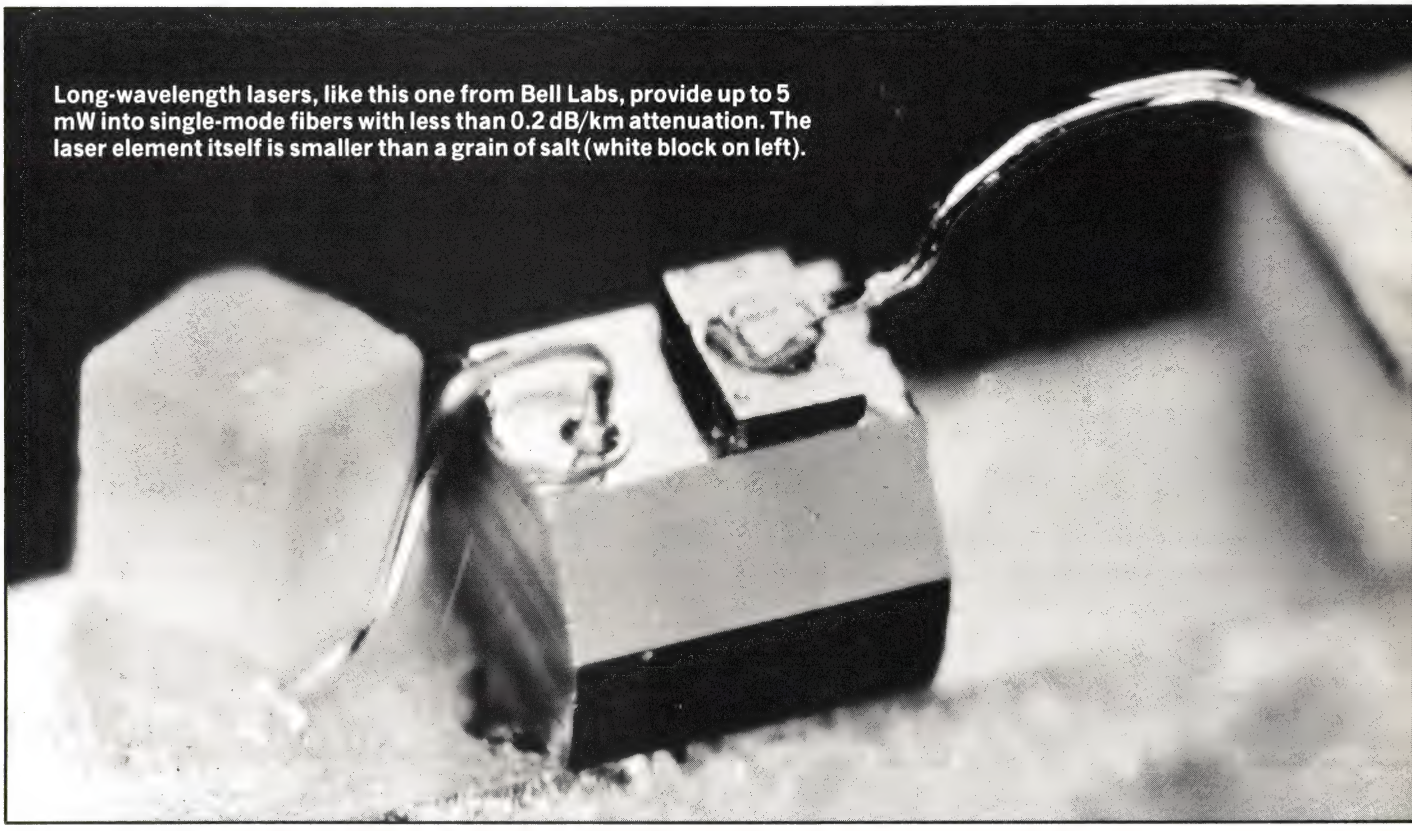
One factor affecting laser operation is the high threshold currents required, typically 200 mA. Extensive development has lowered this threshold. A new series of lasers for 1300-nm transmissions has a forward voltage of 1.5 V and a typical threshold current of just 60 mA, and it produces up to 6 mW. Recently announced by Hitachi America (Arlington Heights, IL), the HLP 5000 series employes a buried heterostructure of InGaAsP on an indium-phosphide substructure. The rise time of the HLP 5000 laser is less than 0.5 nS. The operating temperature range is specified as −20 to +50 C; at room temperature, the laser will provide more than 10,000 hours of continuous operating life.

Another low-threshold laser, operating at shorter wavelengths, is available from Laser Diode Laboratories. The LDL SCW-20 employs a double heterostructure of GaAlAs, for single transverse-mode injection. A threshold current of 60 mA is typical for 7.5-mW output power at 830 nm.

Though intended for short-haul transmissions with a shorter wavelength (typically 800 to 870 nm), the GOLS series lasers from General Optronics (South Plainfield, NJ) will produce a 5-mW output with 1.5 to 2-V forward voltage.

Threshold current is affected by increases in room temperature even within a device's rated temperature; lasers tend to be very sensitive to changes in temperature. A large heat sink for the laser element helps to control this sensitivity to temperature. Another approach is to bombard the light-emitting cavity with protons, in an effort to alter the crystalline structure of the cavity. These techniques, combined with 100 hours of burn-in testing at 5 mW at 25 C, have produced unusual reliability rating for laser diodes.

For example, the products of General Optronics (like the sealed laser pictured at the left) are warranted



Long-wavelength lasers, like this one from Bell Labs, provide up to 5 mW into single-mode fibers with less than 0.2 dB/km attenuation. The laser element itself is smaller than a grain of salt (white block on left).

for 10,000 hours at full power. Based on tests conducted over tens of thousands of hours, the projected life of a General Optronics laser is more than 100,000 hours. LDL has similar lasers for long wavelengths, warranted for 10,000 hours.

Lasers vs LEDs

Though lasers have shown tremendous improvements in reliability, they still have a shorter operating life and much higher price than LEDs. LEDs are most frequently used for transmitting data with shorter transmission lengths. They are protected from variations in temperature by hermetic sealing, which is not always available with laser models. Unlike lasers, they have good transient and overload protection. Substantial differences also exist in typical power outputs.

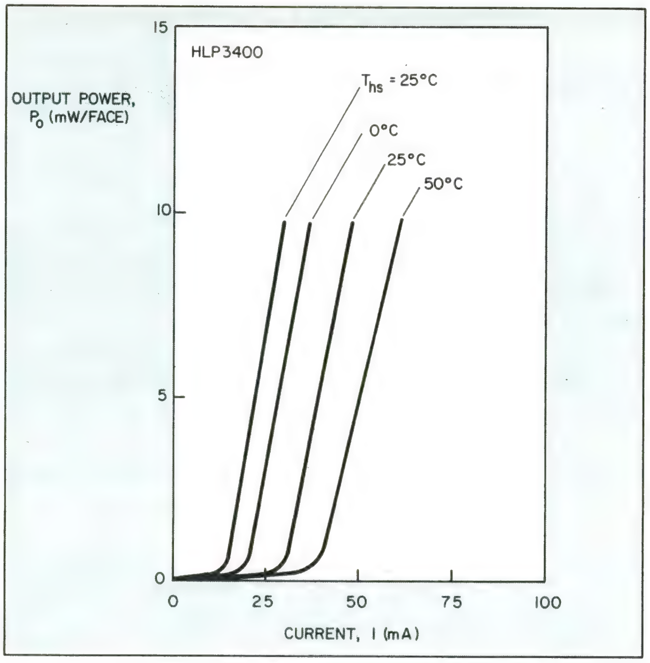
Lasers are noted for their high power output. Pulses up to 3 A with 5 V of forward voltage will produce outputs up to 0.65 W, with less than 1 ns rise time, even at a peak wavelength of 1200 nm. The typical cw laser will put out 5 mW with 200 mA at 1.5 V, but the typical LED will put out a maximum of 0.5 mW with the same driving power.

Most LEDs make use of the GaAlAs technology and operate at visible or near-infrared wavelengths. The most popular LEDs provide from 100 to 500 μW with 200 mA currents, at wavelengths from 700 to 900 nm. Rise time of 5 to 20 ns are typical.

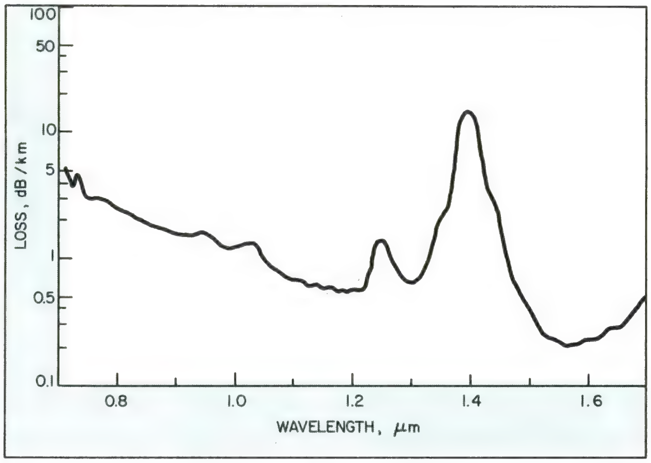
LDL's IRE 160 series provides 200 μW with 100-mA current at 2-V forward voltage. The TXES 400 series of Texas Instruments (Dallas, TX) provides up to 200 μW at 850 nm within 8 ns. Motorola's (Phoenix, AZ) fiber-optic active components put out up to 250 μW in 15 ns with 200 mA. Most LED emitters are designed to sell for less than \$50, with the exception of LDL's IRE-160 (\$200). These devices are perfectly suited for data transmissions at rates below 30 Mbits/s, and over transmission lengths of less than 1 km.

For even higher power outputs, the structure of $Ga_{1-X}Al_XAs$ hemispherical emitting surfaces may be varied to construct LED devices that can put out between 20 and 40 mW at 715 to 905 nm, with 250-mA drive current. Hitachi's IRED high-power LEDs use a domed and "quasi-heterostructure" of GaAlAs, in which the photo-generating pn junction is etched by liquid phase epitaxy. Special packages, including TO-46 cans and heat sinks, ensure the life of the product over the operating range from −40 to 60 C.

The heterostructure formation can also be used to increase the wavelength for longer cable runs. For example, LED emitters from Varian (Palo Alto, CA) provide a typical LED output of 0.5 mW, but also a not-very-typical peak wavelength of 1050 or 1350 nm. With variations in the alloy composition, the optimum dispersion for transmissions in silica fibers occurs at 1270 nm. These light sources provide the longer wavelengths needed for telecommunications; and,



Laser output will shift with temperature. Special heat sinking and hermetic sealing improve the temperature stability and prolong the laser's life.



Optical-transmission losses peak at 1400 nm in single mode fibers used in the far-infrared region. Minimum losses occur at about 1300 and 1500 nm. Some of the most sophisticated systems, as a consequence, are designed for 1550 nm.

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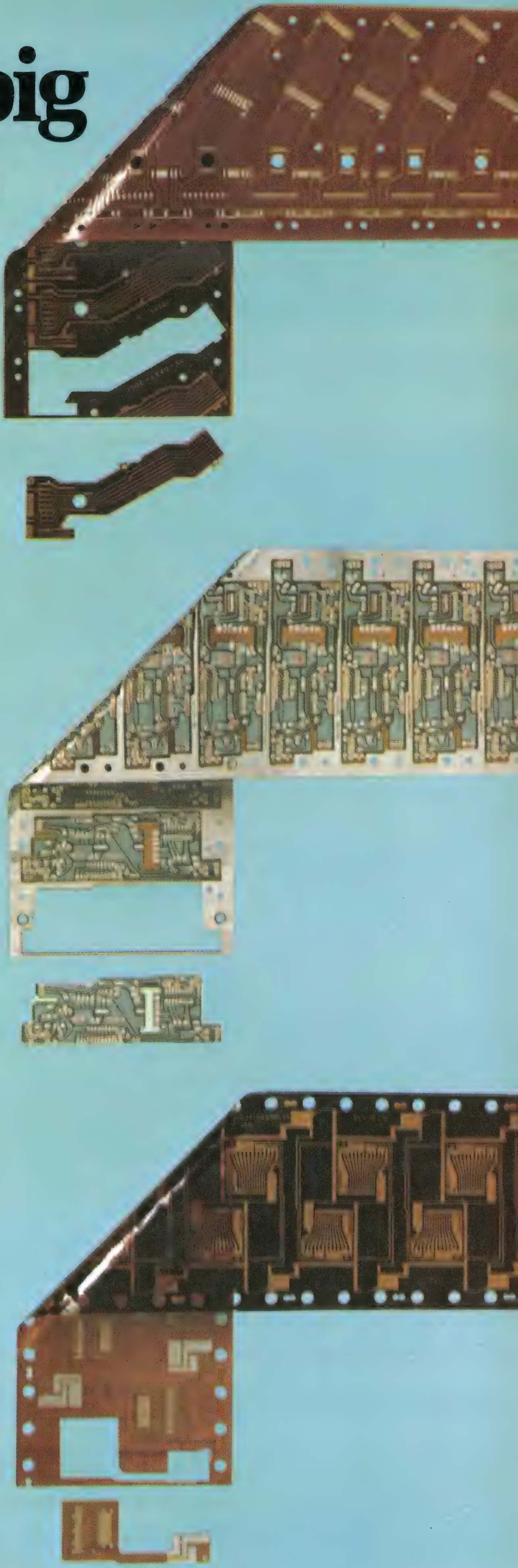

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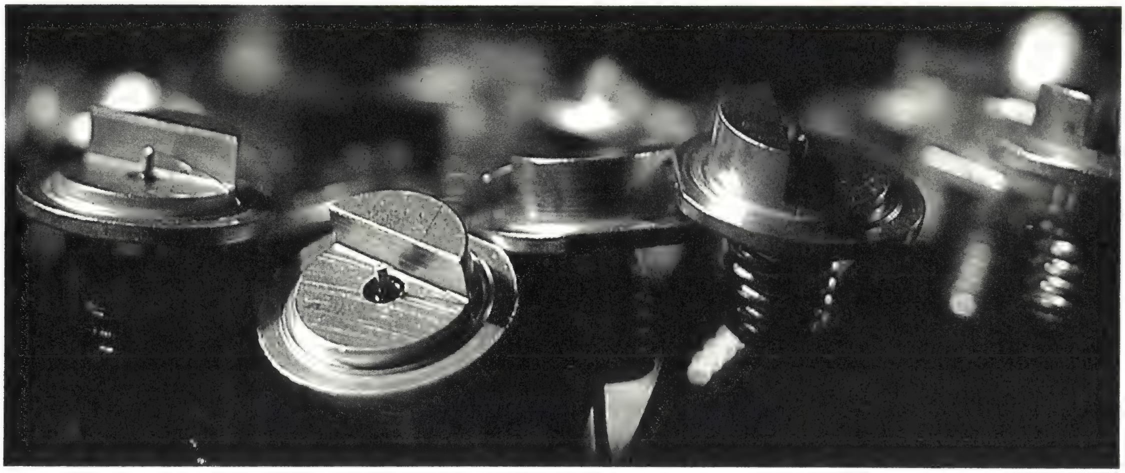


Metal packaging acts as heat-sink material and is among the manufacturing techniques used by Laser Diode Laboratories to lengthen operating life. LDL's lasers are warranted for 10,000 hours.

since they consume less power, they can carry much-needed reliability into the field.

Since most LED devices use GaAlAs technology, the LED emitters employing a InGaAsP matched-lattice, double-heterojunction indium-phosphide can safely be called "second generation LEDs."

New detectors

The progress in long-wavelength emitters has not been paralleled in long-wavelength detectors. The silicon detectors used in p-i-n photodiodes appear to be limited to wavelengths shorter than 1100 nm. As a consequence, many researchers have been considering the use of avalanche photodiodes using germanium. Though they produce high dark currents and considerable noise in the avalanche mode, germanium diodes can provide much needed gain—typically better than 100. Other researchers believe that GaAs FETs will be an effective answer to the problem.

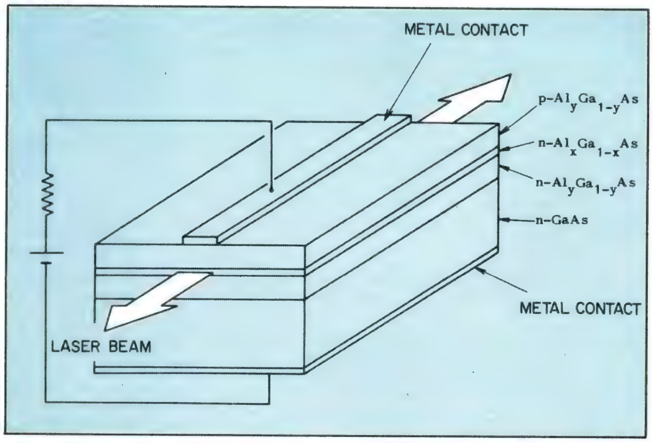
Many researchers consider the ideal detector to be a silicon photodiode combined with a low-noise amplifier on the same chip. Two models of FOAC integrated detectors from Motorola, which operate in 800-850 nm region (the MFOD 402F and the MFOD 403F), provide a p-i-n photodiode on the same chip with a low-noise op amp for a significant voltage output with small variations in light input. The 402 provides a responsivity of 1.0 mV/μW; the 403—first announced at the Fiber Optics Conference in Chicago last September (ELECTRONIC DESIGN, Oct 11, 1979, p. 29)—provides a clean 5.0-mV/μW.

Other detectors from Motorola include p-i-n photodiodes with responsivity rates of 0.20 and 0.40 μA/μW, a photo (npn) transistor package with a responsivity of 100 μA/μW, and a photo Darlington detector with an output of approximately 2800 μA/μW.

Silicon photodiodes from Texas Instruments are designed to operate in the reverse bias mode. High resistivity silicon is used to provide good responsivity —typically 0.3 μA/μW—with low capacitance and at low voltage.

Hewlett-Packard (Palo Alto, CA), the Spectronics Division of Honeywell (Richardson, TX) and Meret Inc. (Santa Monica, CA) are among the manufacturers who are integrating detectors with the driver circuitry as well as with amplifiers. These new low-profile detector packages include complete receivers with TTL-compatible outputs.

Hewlett-Packard's five-pin HFBR-2001 optical receiver package has a sensitivity of 0.8 μW and provides a pulsed output of 2.85 V. Spectronics' SPX 4141 receiver module has a sensitivity of 4 μW, and trans-



The double heterojunction (DH) structure of Hitachi's laser diodes ensures that a high concentration of active carriers are injected into the thin n-$Al_x Ga_{1-x}$ As layer, which can act as an optical waveguide between the sandwiching layers at laser wavelengths.

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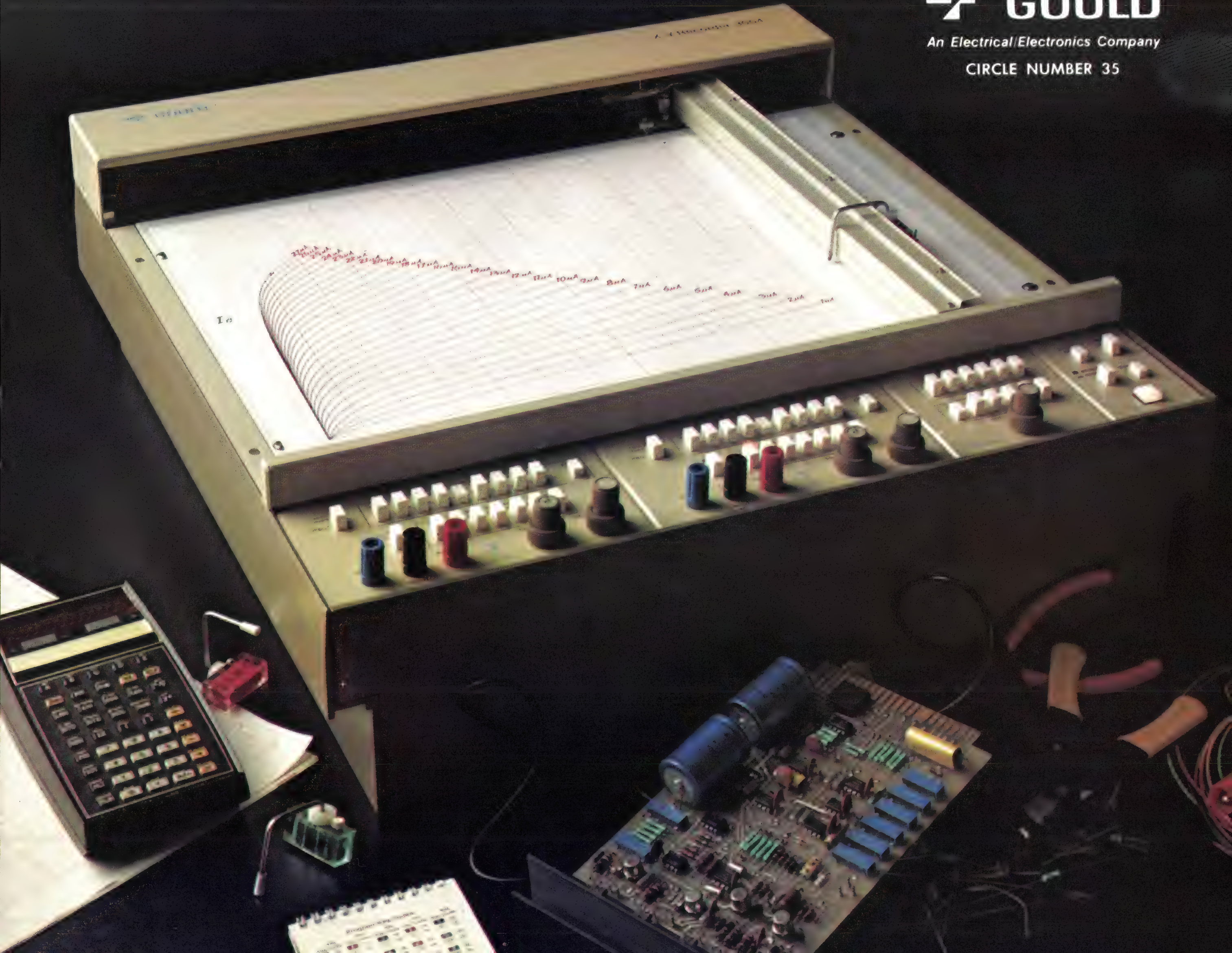


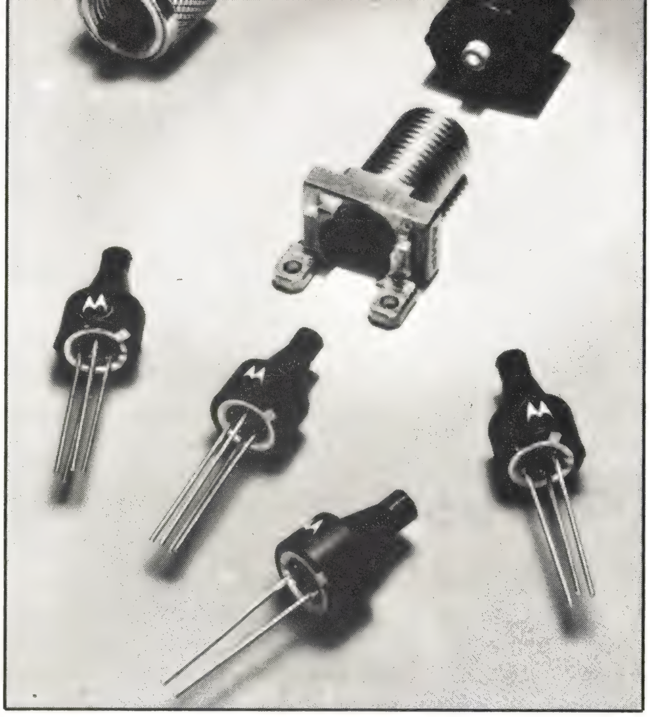
a 25-MHz output, with a 10^{-10} bit-error rate.

Packaging concepts

Hermetic sealing not only prolongs emitter and detector life, but also directs the light efficiently into the fiber—even at shorter wavelengths.

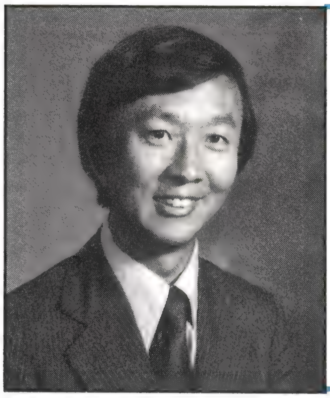
One of the most popular packages is the modified TO-46 can. The laser or LED is mounted inside the can, with a small lens assembly at the top. When mounted into a connector housing—typically a modified SMA-type connector—the lens assembly directs the light into the fiber-optic cable.

A similar approach is taken by Spectronics (Richardson, TX), in the construction of its fiber-optic links and by Laser Diode Laboratories in its "etched-well emitter." Both the transmitter and the receiver modules employ a window assembly at the face of the TO-46 container emitter and the p-i-n photodiode detector. Within the emitter, a high-index glass sphere is mounted in direct contact with the planar LED chip. The sphere collects much of the light that would ordinarily be lost from the surface of the chip, and projects it onto a 300-μm "sweet spot" on the surface of the device window. (This spot is approximately 45 mil in diameter, in Laser Diode's similarly packaged IRF 161 etched-well emitter.)



Emitter and detectors from Motorola are packaged in AMP plastic connector ferrules, a low-cost and effective means of sealing the devices and connecting them with fiber cables. Motorola's new detectors include built-in single-chip preamps.

Emitters and detectors—4 perspectives



"Injection laser diodes emitting in the 0.85-μm region could get substantially less costly soon."

Charles Kao

Charles Kao, vice president and chief scientist of ITT's Electro-Optical Product Div. (Roanoke, VA), has good reason to smile. All the elements of fiber-optic transmission have finally come together—enough to prompt Dr. Kao to state simply, "Fiber-optic technology has passed into the product stage." It's been a long time coming for the man who, back in the 1960s at ITT's Central Research Lab in England, predicted that optical-fiber waveguides would one day be viable media for transmitting information.

Since the, all fiber-optic transmission system components have improved dramatically: For one thing, fiber loss has long since passed the 20-dB/km goal that signaled the medium's practicality. In addition, graded-index cores now all but neutralize once-troublesome modal dispersion. Cabled fibers on the market commonly lose only 3 to 8 dB/km, Kao adds, while providing information bandwidth-distance products ranging from a few MHz·km to 1 GHz·k. And all the while the cost of such high-performance telecommunications fiber has been dropping steadily.

Solid-state light sources are maturing fast—especially in reliability. Chances are good that both injection laser diodes and LEDs of gallium aluminum arsenide, emitting at the popular wavelengths of 0.82 and 0.84 μm, will reach 1-million hours of operation. Kao considers million-hour LEDs a certainty and is highly optimistic that laser lifetimes will reach this level for room-temperature operation. He also concedes that these source-lifetime projections are speculative at this point — not enough time has passed since the devices were introduced.

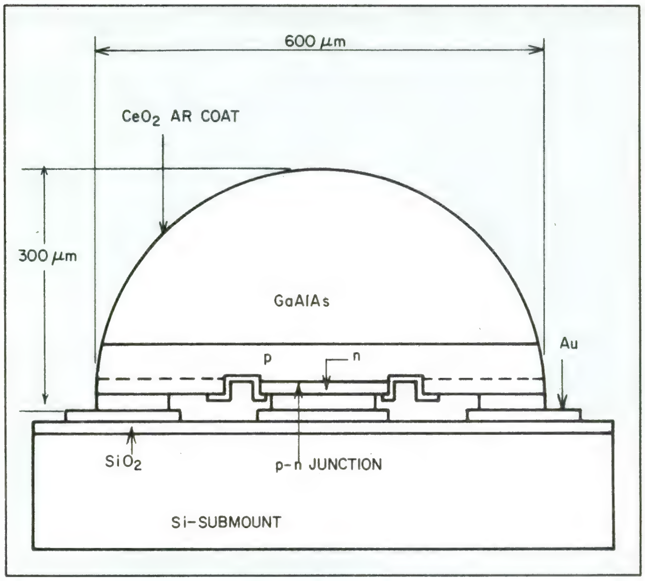
Still, Kao is optimistic about one thing that will affect fiber-optic use in telecommunications: cost

The optical fibers are brought in close proximity with the sweet spot on the window. The sweet spot is most advantageous when used to connect cables with core diameters exceeding 200 μm. With a cable that has a core diameter of 100-μm, the losses in coupling the cable to the sweet spot are about 3 dB greater than with the pigtail approach.

The pigtail approach is used in many of the emitter products from Laser Diode Laboratories and in emitters and detectors from Texas Instruments. The end of a fiber with a core diameter of 400 μm is glued directly to the light aperture of a LED emitter. The light emerging from the opposite end of the fiber length is coupled directly to the end of a mating fiber-optic cable. Coupling losses are controlled by matching the numerical apertures of the mating fibers.

Metal-cases and plastic DIPs are among the packaging options available with Texas Instruments' sources and detectors. The epoxy-filled metal-package is similar to the JEDEC TO-5 outline; the 6-pin DIP package is intended for PC-board mounting.

A variation of the pigtail approach is the packaging scheme used in Motorola fiber-optic emitters and detectors. The pigtails are short cables that have a core diameter of 200 μm. The semiconductors and their pigtails are packaged in plastic connector ferrules provided by AMP (Harrisburg, PA). When mounted in a specially designed connector housing, the ferrules ensure precise end-to-end mating of the fiber elements. Alignment angles are controlled.■■



The high-power infrared emitting diode from Hitachi uses a forward biased pn junction to push photons into the GaAlAs crystal dome. The concentration Al controls the wavelength, and promotes strong emissions.

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considerations. "Though injection laser diodes emitting in the 0.85-μm region currently cost hundreds and even thousands of dollars each, these GaAlAs devices have a great chance of getting substantially less costly soon," Kao says. That is because this type of laser is being used in video-disk playback systems. If such home units become popular, Kao figures a great many lasers will be needed—perhaps millions. Then the usual economic benefits resulting from large-scale production should lower unit costs dramatically. "Laser diodes, after all, are not too different from other semiconductor devices," Kao explains.

Warming to the subject of telecomm-cost considerations, Kao advises that transmitting signals over the longest span possible without repeaters usually produces the lowest-cost systems. In fiber-optic spans, this translates into launching the maximum amount of light into the fiber and detecting the resulting signal at the far end with the most sensitive device.

Lasers launch more light than LEDs because of higher output and more efficient coupling. Kao suggests the following rules of thumb: Typical lasers couple up to 1 mW of optical power into the 50-μm core of a standard graded-index telecommunications fiber; typical LEDs launch 10 to 13 dB less. Hence, the type of source alone can account for over 4 to 20-km difference in telecomm transmission span.

However, for spans short enough to have optical power left over, Kao leans toward LED sources because of their currently higher reliability and lower cost. For moderate-bandwidth analog transmission, too, he prefers LEDs, because they are easier to modulate linearly.

For 50-Mbit/s data rates and beyond, Kao advises looking to lasers, but cautions that since a laser is a coherent source, laser systems can be subject to multipath problems, similar to the multipath fading that nettles microwave-system designers. This prompts him to point out that increased power alone is not always the answer—experienced designers consider the side effects. For this reason, ITT researchers in England paid a lot of attention to the multipath phenomena that occurred in 50-μm-core, graded-index fibers. They even came up with a name: modal noise.

Silicon avalanche photodiodes have become the most sensitive detectors in the 0.85-μm range. But Kao also notes that recent practical and theoretical demonstrations have shown a pin-diode detector followed by a low-noise FET amplifier to have almost comparable sensitivity.

Having observed fiber optics pass into the application stage, Kao is not content to discuss currently available components, but looks to future systems using tomorrow's products. Today, in interoffice trunking of telephone traffic, most fiber-optic spans are less than 10 km. Reaching for longer than 10 km of repeaterless transmission requires lower fiber loss than 0.85-μm operation provides. Citing cable losses of 1 to 2 dB/km in the long-infrared wavelength range from 1 to 1.6 μm, Kao envisions resulting repeater spacings stretching to 20 km or even longer.

Looking into the future and making predictions are two different things, however. Though he thinks a long-wave pin-diode detector and a GaAs FET amplifier could make a highly sensitive optoelectronic receiver, Kao is not very hopeful about long-wave IC transceivers. Such monolithic devices would need an implanted emitter and detector, which in turn would require selective epitaxy because the required dopant levels and material systems are so different for each section. Even an IC version of a long-wave receiver seems beyond possibility for now to Kao. But he does foresee practical hybrid long-wave receivers.

When emitters do become available for generating many separate wavelengths, fiber-optic transmission systems should provide enormous information-handling capacity via wavelength multiplexing. Kao envisions separate sources that emit wavelengths spaced about 100 A apart being launched into one fiber through wavelength-dependent couplers. At the receiving end, he envisions wavelength-dependent couplers demultiplexing the multiwavelength carriers. Such an "optical FDM system" would allow an installed fiber system to be expanded in steps.

Finally, the low theoretical loss already credited to fibers, encourages Kao to look well into the future and envision products of what appears to be the exponential growth of fiber-optic technology: repeaterless spans stretching across oceans. No wonder Charles Kao is smiling now.

"At near-IR wavelengths, silicon technology can deliver just about anything needed for an optoelectronic receiver."

Harry Koski

Fiber-optic semiconductor technology is now squarely into the second product generation. Not only that, but "with today's products and those about to be introduced, fiber-optic transmission will not only outperform wire in many commercial computer and industrial applications, but it will cost less." That's what Harry Koski, optoelectronics manager at Motorola (Phoenix, AZ), believes.

Part of this new generation are what Koski describes as "new-wave" optoelectronic detectors that combine pin-diode detectors and a preamplifer on one silicon chip, rather than use silicon discrete photodetectors with separate amplifiers. Though high internal gain makes one type of photodetector, the silicon avalanche photodiode, extremely sensitive, Motorola prefers pin-diode detectors, which, Koski says, can be easily integrated while APDs cannot. One reason is that pin detectors operate from low-voltage supplies, APD from high.

Pin diodes themselves develop little noise but are low-gain devices that require substantial amplification to be useful. Preamplifier noise—especially the pickup along the input lead—usually overshadows pin-detector noise. But in the second generation, integrating a pin device and a low-noise preamplifier obviously reduces the input lead length and associated noise problems. "In addition to the noise benefits and the obvious cost benefits, we have been able to obtain higher data rates by integration," Koski notes.

"IC detectors have surpassed the 20-Mbit/s data-rate barrier in computer interconnection: 40-Mbit/s rates are available routinely," Koski states flatly. He also notes that because pin-type structures have inherent high speed and monolithic receivers have such short lead lengths and low stray capacitances, even higher data-rate operation will become practical. Using an IC detector, one computer manufacturer has already reported 100 Mbits/s.

Now that the practicality of the IC detector has been nailed down to Koski's satisfaction, more members of the family will follow shortly—in particular, a complete one-chip receiver that will convert input optical energy to a TTL output. With the postamplifier added to the chip, the number of leads will go down to three. This further reduces the cost of manufacturing fiber-optic interfaces.

Reducing the number of leads is particularly important in Motorola's IC receiver because a ferruled version is intended to work with the Fiber Optic Active Connector system developed jointly by Motorola and AMP. An inexpensive and reliable system for precisely joining fiber and semiconductor, the FOAC requires the leads to be bent onto the retaining PC boards. So the fewer the leads, the better.

Koski freely admits that the IC receiver, sensitive as it is, won't solve all data-transmission problems. "Ultrahigh-speed systems, of course, still require lasers and APD," Koski concedes, "but simpler and less expensive devices can handle most applications." Koski emphasizes that cost effectiveness need not stand in the way of performance goals in most applications: "At near-infrared wavelengths, silicon technology can deliver just about anything needed in the way of an optoelectronic receiver."

(continued on page 62)

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ED2 1/80

"Better fiber-optic parts take the heat off LEDs, raising emitter lifetime exponentially."

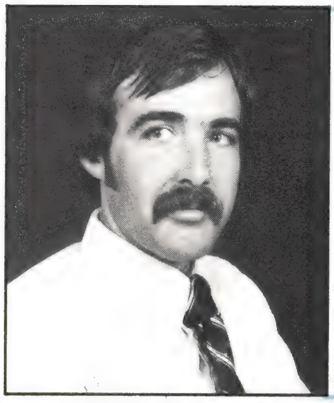
David Medved

For sources in the 800 to 950-mm range, David Medved prefers LEDs to lasers, provided they meet the required total optical-attenuation · bandwidth product. "LEDs cost less and are more reliable than lasers," says the president of Meret (Santa Monica, CA). He sorts LEDs into three general price/performance ranges: Simple surface-emitting LEDs costing as little as $5 inject 20 to 30 μW of optical power into a step-index fiber at up to 1-Mbit/s data rates. Domed LEDs costing $25 to $30 inject about 200 μW, when properly centered to a step-index fiber, at over 20 Mbits/. Integrated optical sources, like Spectronics' Sweet Spot (around $100) and pigtailed edge-emitting or etched-well Burrus-type LEDs (between $150 and $300) inject 50 to 100 μW into a graded-index fiber at 50 Mbits/s.

Characterizing a link as either terminal or cable-dominated in price, Medved considers typical process-control links with 30 to 100-m spans usually terminal-dominated because more than half the total system cost goes into transmitter and receiver terminals. Obviously, emitter cost is significant here. However, when future telecomm links span 10 to 20 km by using long-wave technology, Medved says even $1000 might not be too much to pay for the source.

At the other end, with well-designed receivers operating acceptably with input power threshold levels of 2 μW—even at high data rates—Medved concludes that the most inexpensive surface-emitting LEDs usually can handle 10-Mbit/s process-control links stretching 30 to 100 m. At even higher data rates, a $30 dome-type LED can launch 200 μW into a cabled fiber whose attenuation is 8 dB/km. The resulting 20 to 30 dB of fade margin translates into 4 to 5 continuous kilometers of cable. Medved favors centering LEDs to fibers at the link factory where ten minutes of tweaking can save significant cost.

Another Medved recommendation: Operate LEDs well below their rated power level. Rather than hit a diode with the normal 100 to 200 mA that is half the absolute max rating, run an emitter with only 20, 30 or 40 mA. Lifetime will go up exponentially—a 20,000-hour diode should surpass 200,000 hours if its 100-mA drive is reduced to 20 mA. And what a boon to battery operation.



"Pigtailed sources and detectors can be placed anywhere on the board."

Dennis Smith

There are several popular ways to bring a fiber-optic signal from a PC board to a cable—but good reasons for using pigtails, according to Dennis Smith, manager for fiber-optic systems at T&B/Ansley (Los Angeles, CA).

With pigtailing, semiconductor sources and detectors can be placed anywhere on a board, without preventing the pigtail ends from merging into one common I/O port. In addition, pigtailing provides a low-cost connection with repeatable insertion losses.

"It would be difficult to make a sensible multichannel fiber-optic connector without using pigtails," Smith asserts. Where individual semiconductor elements are integrated with the connector body, for example, it would be difficult to construct a multichannel I/O port without putting together an impossibly massive connector.

But what about harnessing a large-diameter pigtail to a small-diameter cable fiber? Insertion losses would be large: For example, a plastic-clad silica fiber with a 200-μm core diameter receiving light from a pigtail with a 400-μm core diameter will produce typical losses of 8 or 9 dB. These signal losses, however, can be easily tolerated for transmissions of less than 1 km. Therein lies the primary advantage of pigtailing, according to Smith: It is cost-effective for most short-haul applications.

Insertion losses could be reduced by matching the pigtail's numerical aperture to the cable fiber. But then the connector would be more complicated and probably cost more, Smith believes.

Large pigtails, in contrast, can tolerate up to 100-mil variation between core and cable-fiber diameters and still produce the same insertion loss. This means that the connector tolerances can be much broader. As Smith notes, "You can figure your connector costs to be very small, and you'll always get a repeatable connection."

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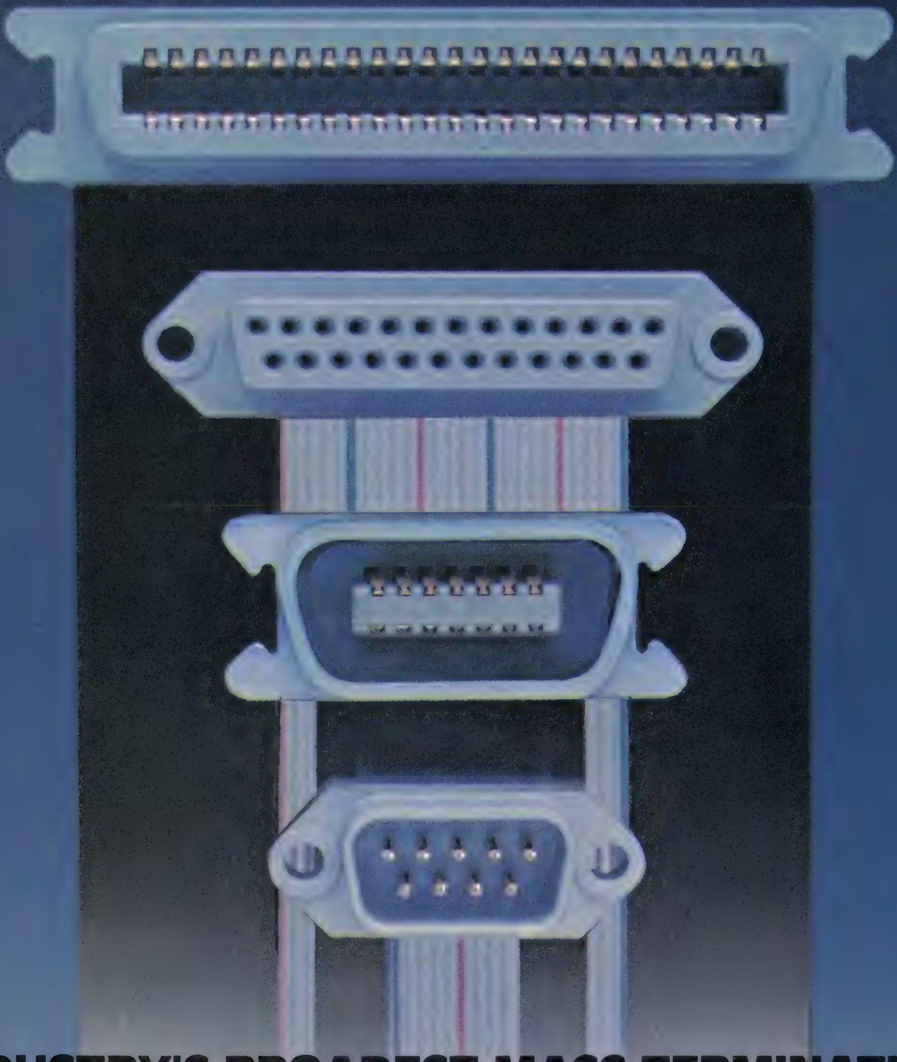

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And these "D" connectors mass terminate without wire stripping or soldering to all types of BLUE MACS® flat cable, including round conductor cable, and jacketed and shielded jacketed flat cable, designed and U.L. listed for external interconnections.

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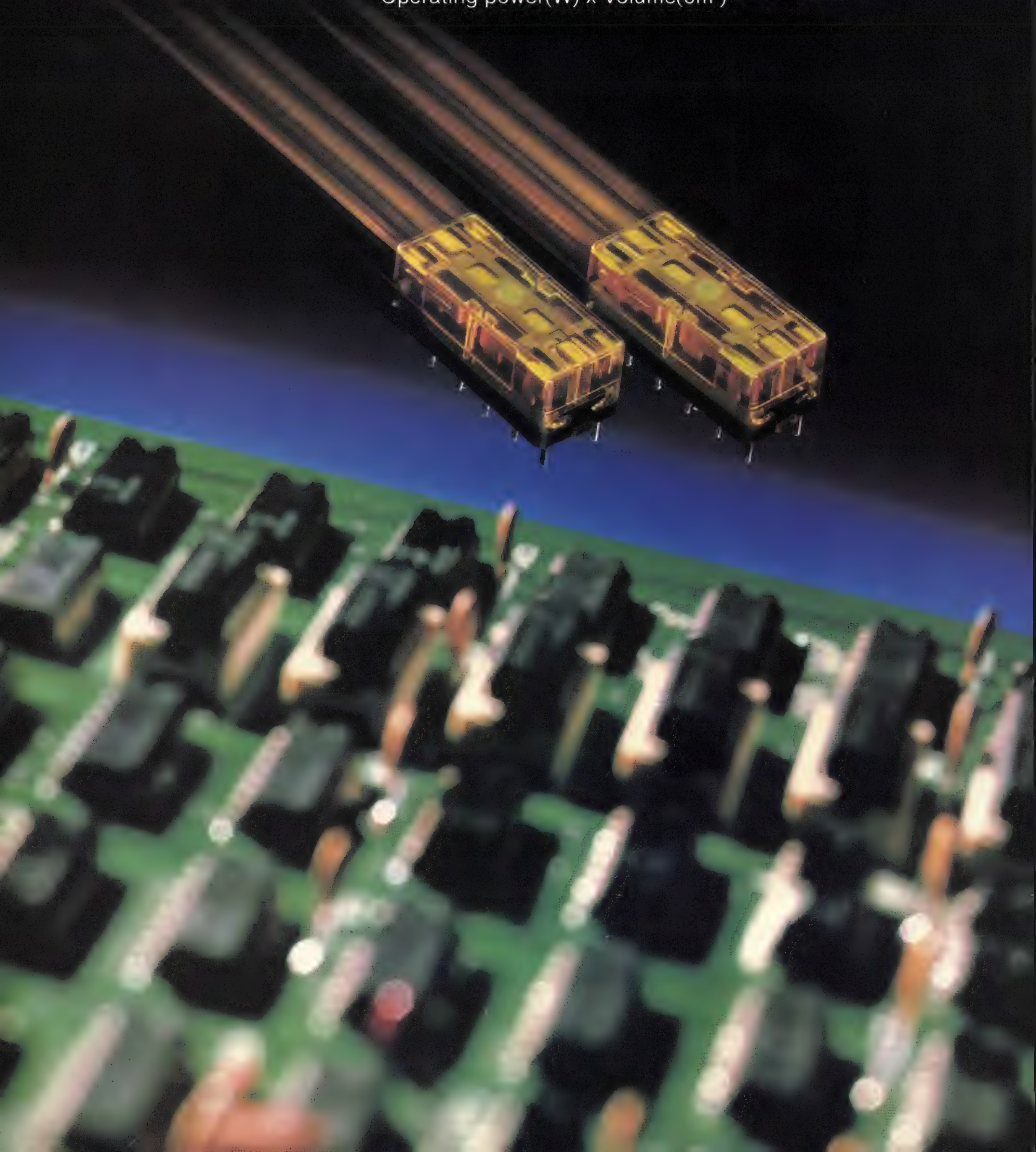
CIRCLE NUMBER 37

Aromat SE Amber Relays... a pure product of "relay efficiency."

$$\text{Relay efficiency}(\eta) = \frac{\text{The sum of all contacts' switching capacity (VA)}}{\text{Operating power(W)} \times \text{Volume}(\text{cm}^3)}$$



A breakthrough in relay efficiency.

The SE Amber relay's key to higher efficiency lies in greater miniaturization coupled with high reliability and greater switching capacity.

- **High sensitivity in small size.**
  [Operating power (W) x Volume(cm^3)]

The SE Amber relay's 4-gap balanced armature delivers a highly efficient polarized magnetic circuit—sensitive enough to be driven directly by an IC, in a space 28L x 12W x 10H mm.

Sensitivity

Pick-up power	100 mW
Nominal operating power	200 mW

Dimensions

Volume	28L x 12W x 10H mm 1.102 x .472 x .394 inch	
Header area	$336mm^2$	.521 $inch^2$
Height	10mm	.394 inch

- **Wide switching range.**
  [The sum of all contacts' switching capacity (VA)]

Switching is possible from 100μA 100mV DC to 4A 250V AC, thanks to the 4-gap balanced armature system and special multi-layer clad contacts. A single SE relay can handle maximum and minimum switching simultaneously.

- **High reliability and long life.**

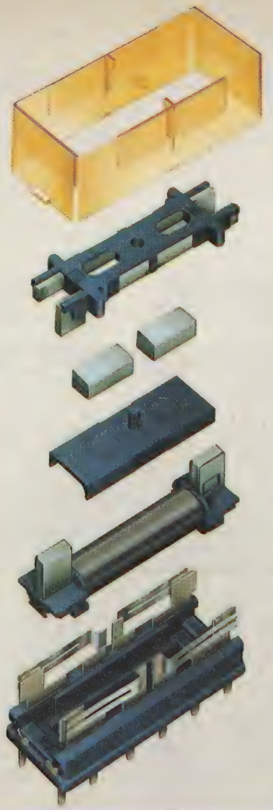
The balanced armature system with permanent magnets gives larger contact pressure. Bifurcated contacts and lower contact bounce add to contact reliability and expected contact life.

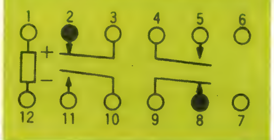
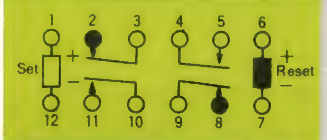
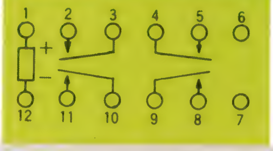
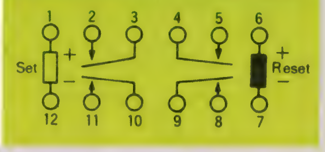
- **Amber design and construction.**

Designed for automatic wave soldering and cleaning, the sealed SE Amber relay performs reliably under conditions where hydrogen sulfide, silicone and ammonia fumes prevail.

- **High vibration/shock resistance.**

The balanced rotating armature provides great resistance to shock and vibration. Vibration resistance: 10 to 55G (amplitude: 3mm) Shock resistance: 50G (11msec.).



	Single side stable (De-energized position)	**2 coil latching** "Reset" position when reset coil is energized with indicated polarity.
2a **2b**		
4a		

- **Varied contact arrangement.**

SE relays are available with bifurcated contacts in 2a2b and 4a contact arrangements.

- **Multiple latching.**

2-coil latching types are available, in addition to single side stable types.

Since SE relays have a latching capability with multiple contacts, one contact can control the circuit while the other can switch the load simultaneously.

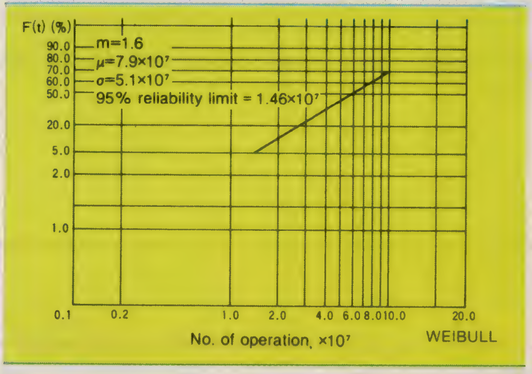
- **Low thermal electromotive force.**

Because the SE relay has completely separate coil and contact chamber areas, extremely low thermal electromotive forces are possible.

- **Dual in-line package arrangement.**

This 2-track terminal arrangement allows easier component insertion, easier layout and identification of terminal locations, and simpler in-line checking.

Contact reliability Test condition: DC1V/1mA, 4 contacts in series Detection level 10Ω Sample: S4E-24V Q'ty = 10



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CIRCLE NUMBER 40

Bilingual, 16-bit μP summons large-scale computer power

Aided by advanced architectural concepts, a 16-bit microprocessor can measure up to a large-scale computer, with multitasking, memory management of 16 Mbytes and peripheral control. Fabricated from XMOS technology, the NS16000 family of CPUs shows how: The 64-kbyte address spaces of the 16008 can be upgraded to the unsegmented 16 Mbytes of the 16032. Then, with the addition of a memory management unit (MMU), the unsegmented address spaces of the NS16016 and 16032 can be upgraded even further to 32 Mbytes (see Table 1).

The unsegmented memory and uniform addressing permit users to build libraries of ROM-based software. A bilingual instruction capability (native and 8080 emulation) and slave processors that are transparent to the software provide enhanced performance, equal to that of many large minicomputer systems. Additionally, the native instruction set, with its powerful addressing modes, readily accommodates structured high-level languages, to ease the programmer's burden.

Programming for the NS16000 family is easy and efficient because the architecture is symmetrical with respect to registers, instructions, data and address modes. Symmetry in the registers and in the data means that all eight, general-purpose registers and several types of data (see Table 2) look the same to the instructions. Thus, for example, the instructions can use any register for any purpose, whether as an accumulator, as a base register or as an index register.

Instructions: powerful and symmetrical

Because the instructions are symmetrical, every register reponds to every instruction. Similarly, every instruction can make use of every relevant addressing mode. Finally, symmetry between the registers and memory means that each memory location can serve as an accumulator or base register, as needed, expanding the number of registers available.

All processors in the NS16000 family have a native set of 100 basic instructions, selected for their frequency of use in different applications. The instructions can use up to five operands; however, most need only two. Efficient programming and compact operation codes result. The instruction set can be expanded by means of slave processors and trap mechanisms.

Inside the top-of-the-line NS16032 central processor are two files. One consists of eight 32-bit general-purpose registers that can be used for either data or address manipulation. The other file contains 24 and 16-bit dedicated registers for storing address and status information.

Both the instruction set and the architecture can handle many types of data—byte, word, double word and strings, arranged into various data structures, as shown in Table 2. Additionally, basic bit-manipulation instructions (such as Test and Set) are included.

Bit fields may be 1 to 32 bits long. Arrays of bit fields and multiple-word bit arrays are easily accessed from a block of memory handled by instructions. The complement of character-string operations includes "translate and compare" and "test for escape character." These instructions are comparable to commands available on large minicomputer and mainframe computers. Also in the instruction set are a complete set of the single-precision (IEEE format) and double-precision floating-point instructions. The

Table 2. Comparison of instruction and data types

Processor	Internal data and ALU bus	Direct address range (bytes)	Address range with MMU
NS16008 (8080 comp.)	16 bits	64 k	N/A
NS16016 (8080 comp.)	16 bits	64 k	32 Mbytes
NS16032	32 bits	16 M	32 Mbytes

Subhash Bal, Product Marketing Manager, NS16000 Family, **George Chao,** Director of Microprocessor Marketing, and **Zvi Soha,** Design Manager, National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051.

mathematics set performs add, subtract, multiply and divide, as well as standard rounding and conversion.

Powerful addressing simplifies programming

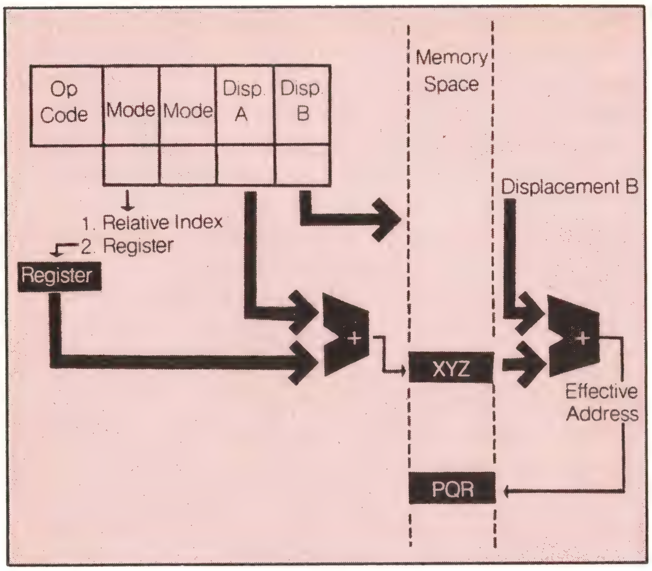
The instruction set employs nine addressing modes, including scaled index (powerful when used with high-level languages), external address (useful in conjunction with modular software) and memory relative (a powerful mode that is seldom available in microprocessor systems). As Fig. 1 illustrates, the memory relative mode involves two displacements—A and B.

Displacement A is added to the contents of a selected register, to point into a memory location. That location contains a memory pointer, XYZ. The value of XYZ is indexed by displacement B to point into the memory locations containing PQR, which is the operand required. The memory relative mode constitutes a very powerful way to handle address pointers and to manipulate fields within a record. In the latter case, displacement B specifies the location of a field in a record pointed to by XYZ. The exact size of the operand PQR is also programmable. This operating mode is actually an extension of indirect addressing.

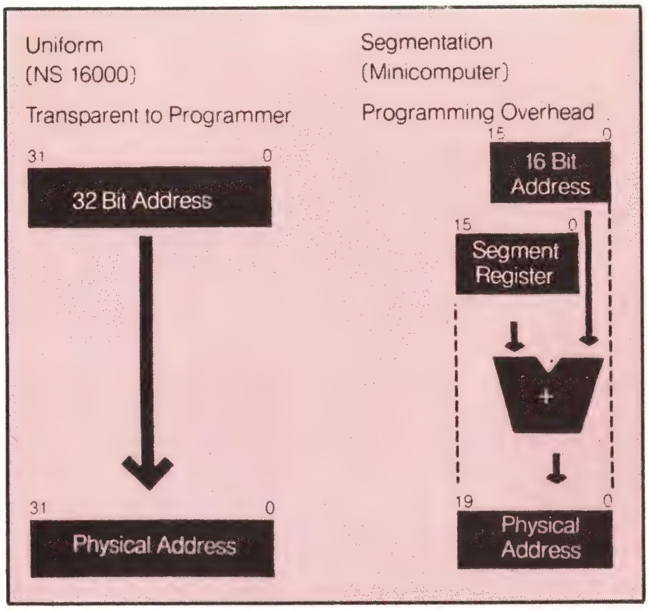
The various addressing modes give the processor considerable flexibility for program development; and a large, uniform address space lets users expand the memory space of a system beyond the 64 kbytes

Table 1. Comparison of NS16000 family processors

	16008/ 16016	16032	8086	Z8000	68000
System structures:					
Virtual architecture		X			
Module map and modules	X	X			
Uniform addressability	X	X			X
Primitive data types:					
Integer byte or word	X	X	X	X	X
Integer double word		X		X	X
Logical byte or word	X	X	X	X	X
Logical double word		X			X
Character strings (byte, word)	X	X	X	X	
Character strings (double word)		X			
BCD byte	X	X	X	X	X
BCD word	X	X			
BCD double word		X			
Floating point	X	X			
Data structures:					
Stacks	X	X	X	X	X
Arrays	X	X			
Packed arrays	X	X			
Records	X	X	X	X	X
Packed records	X	X			
Context mode switching—save block	X	X		X	X
Bit arrays (byte, word)	X	X		X	X
Bit arrays (arbitrary length)	X	X			
Primitive control operations:					
Condition code primitives	X	X		X	X
Jump	X	X	X	X	X
Conditional branch	X	X	X	X	X
Simple iterative loop control	X	X	X	X	X
Subroutine call	X	X	X	X	X
Multiway branch	X	X			
Control structure:					
External procedure call	X	X			
Semaphores	X	X	X	X	X
Traps	X	X	X	X	X
Interrupts	X	X	X	X	X
Supervisor call		X		X	X



1. There are many addressing modes available in the NS16000 processor family. But the memory relative mode offers the programmer great flexibility. The mode not only lets the programmer manipulate records at will, but do the same with pointers.



2. The architecture of the NS16000 CPU family limits the addressing range to 4-billion bytes if the program counter or memory management scheme is expanded beyond the currently used 24-bit width. In older processors that were limited to a 16-bit direct address, segmentation schemes to increase the address space were often used, but they also introduced some delays because of the extra calculations required, and made programming cumbersome.

available with most microprocessors. The unsegmented address space of the NS16000 family can directly access 16 Mbytes of memory.

Many minicomputer manufacturers and some microprocessor manufacturers have adopted the concept of segmentation to expand memory beyond the limitations of a 16-bit address bus. Although segmentation maintains software compatibility and permits memory expansion, the 16-bit limitation restricts segment size. A data structure greater than the segment size cannot be addressed efficiently. Increased overhead is often incurred for software development, memory size and speed, and it is difficult to maintain software compatibility beyond the originally designed address space.

Uniform address space, flexible management

In the NS16000 family, the disadvantages of segmentation have been eliminated by the uniform address space. In the NS16008 and 16016, the 16-bit pointers are upwards compatible to the NS16032 address space via software. The NS16032 has a 24-bit address pointer that can access up to 16 Mbytes without segments.

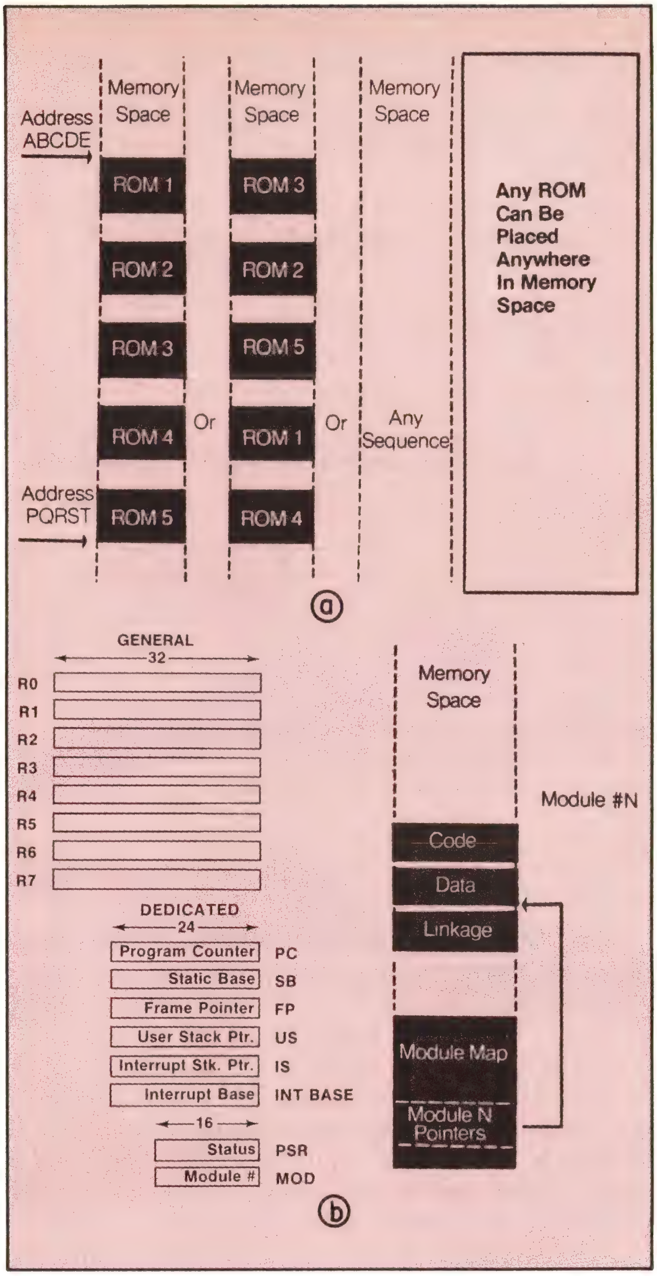
The architectural limit of the NS16000 family is 32 bits, which translates into 4-billion bytes (Fig. 2). As the architecture itself specifies that all memory pointers must be 32 bits long, software compatibility is maintained when memory addressing is increased. Thus, uniform unsegmented addressing provides for a flexible memory management scheme with no added expense.

Since the pointers reach any point within the address space, modular software is easily developed and can be located anywhere within the memory space. With a library of modular ROM software, any software package can be developed independently of all other packages, without regard to individual addressing or linking (Fig. 3a). This capability reduces the cost of production and design.

In several other advanced microprocessors, the modular-software concept has been impractical because the ROM software package must, at linkage time, know the location of the RAM, the external procedures and the services.

Each software module in an NS16000 system contains linking information to the other modules, and a module pointer map held in the module table ties all the modules together. In all CPUs, a MOD register accesses the module table, which functions as a directory. The MOD register contains the index of the module under execution: It points into the section of the module table containing the addresses of the three module components (program page, static data and linkage data, see Fig. 3b).

The external addressing mode uses the linkage information provided by the mapping arrangement. Its external procedure call consists of several commands, two of which include Call External Procedure and Return External Procedure, that switch between program modules. The entire procedure is similar to performing a context switch when a program is running.



3. When relative addressing is combined with a large address range, position-independent programs can be stored ROMs anywhere in the memory space (a). Position-independent software also leads to modular programming, in which independent software modules are linked together via a mapping scheme (b).

```
               MVITW RS, Rb   ; Multiply
              [TO     80      ; Mode switch to 8080
Escape        [
Instructions  [CALL   SAMPLE  ; Assembly code subroutine
              [TO     16      ; Mode switch to NS16000 CPU
               •      •
               •      •
               •      •
SAMPLE         DAD    DE
               RET
```

4. Mixing both the native and 8080 commands requires that the programmer just use one common instruction, "TO," referred to as an Escape command to transfer from the native instructions to the 8080 instructions, or vice versa, if desired.

Bilinguality: the road to compatibility

One of the goals of the NS16000 family is to provide a friendly and gradual transition from existing 8-bit designs to the higher level processors, such as the NS16008 and NS16016. Both of these processors have two instruction modes, a native mode and a direct 8080 emulation.

With the latter mode, a user can run existing 8080 software on the 16008 and 16016 (including ROM-based software on the 16008) and get an immediate fourfold improvement in processing speed. Since the native and 8080 codes can be intermixed, processing speeds increase when the 8080 code is converted to native code.

Further, the native codes of the 16008 and 16016 are fully compatible with the 16032. Thus, the full capability of the 16032's architecture can be gained without a loss of software.

The program in Fig. 4 shows the processor executing a program in the native mode. To switch from the native to the 8080 mode, the programmer uses the ESCAPE instruction. At this point, a subroutine (SAMPLE), which is written in 8080 assembly language, can be executed. At the conclusion of the subroutine, control returns to the main program, another ESCAPE instruction is encountered, and the CPU switches back into the native instruction mode. Unlike a translation scheme, this procedure does not require separate translator and assembly programs.

Slave mode determines execution speed

The architecture of the NS16000 permits the instruction set to be further expanded by special slave processors (Fig. 5). The slave processor may execute a high-level instruction set (working as a floating-point processor, for example) or it may expand upon system-oriented capabilities (working as a memory-management circuit).

The slave hardware and implementation are transparent to software, to ensure that it will be compatible with future system designs and that it will not become obsolete with higher levels of integration.

Under the slave concept, programs are executed at three different rates. The fastest speed is achieved by integration on the processor itself, and the medium speed is obtained when the master processor directs the execution of programs on slave hardware. At the lowest level, with no slave on the bus, the CPU traps its software to a service routine; the software emulates the required operation.

Support circuits for the NS16000 family are in design and will include a memory management unit, a floating point processor, a bus arbiter, a direct-

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Resistance tolerance	±5%
Temp coeff	±100 ppm/°C
Coating	Non-flammable epoxy
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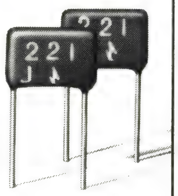
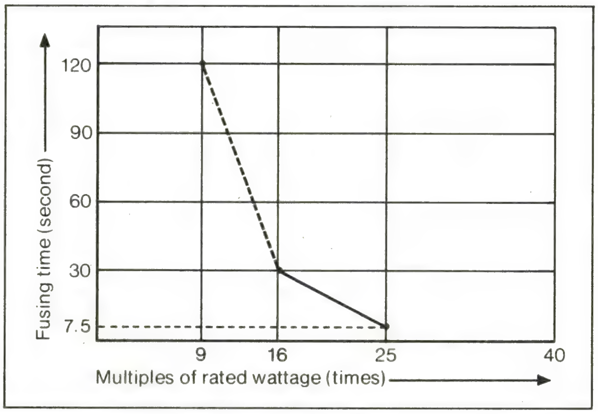
US Patent: 4031497	



Fusing characteristics



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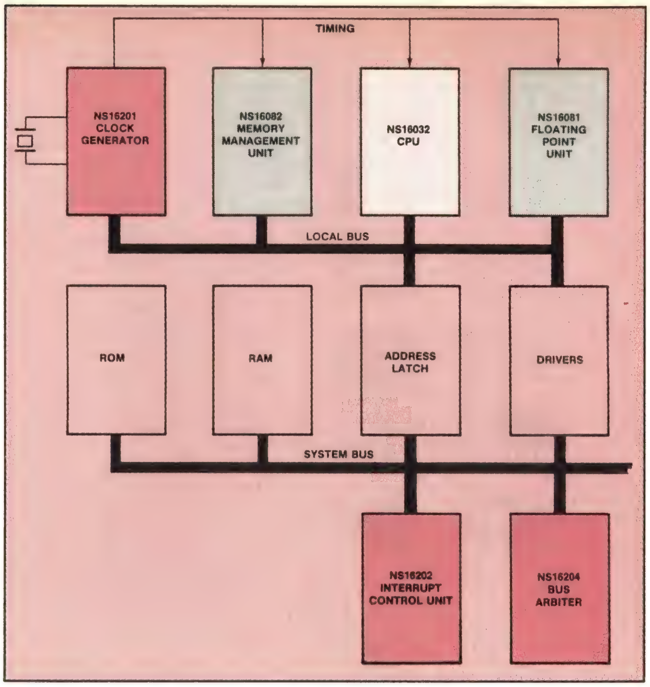


5. The system architecture of an NS16000-based computer shows how the CPU combines with slave processors to add more functionality without losing compatibility as system capability grows.

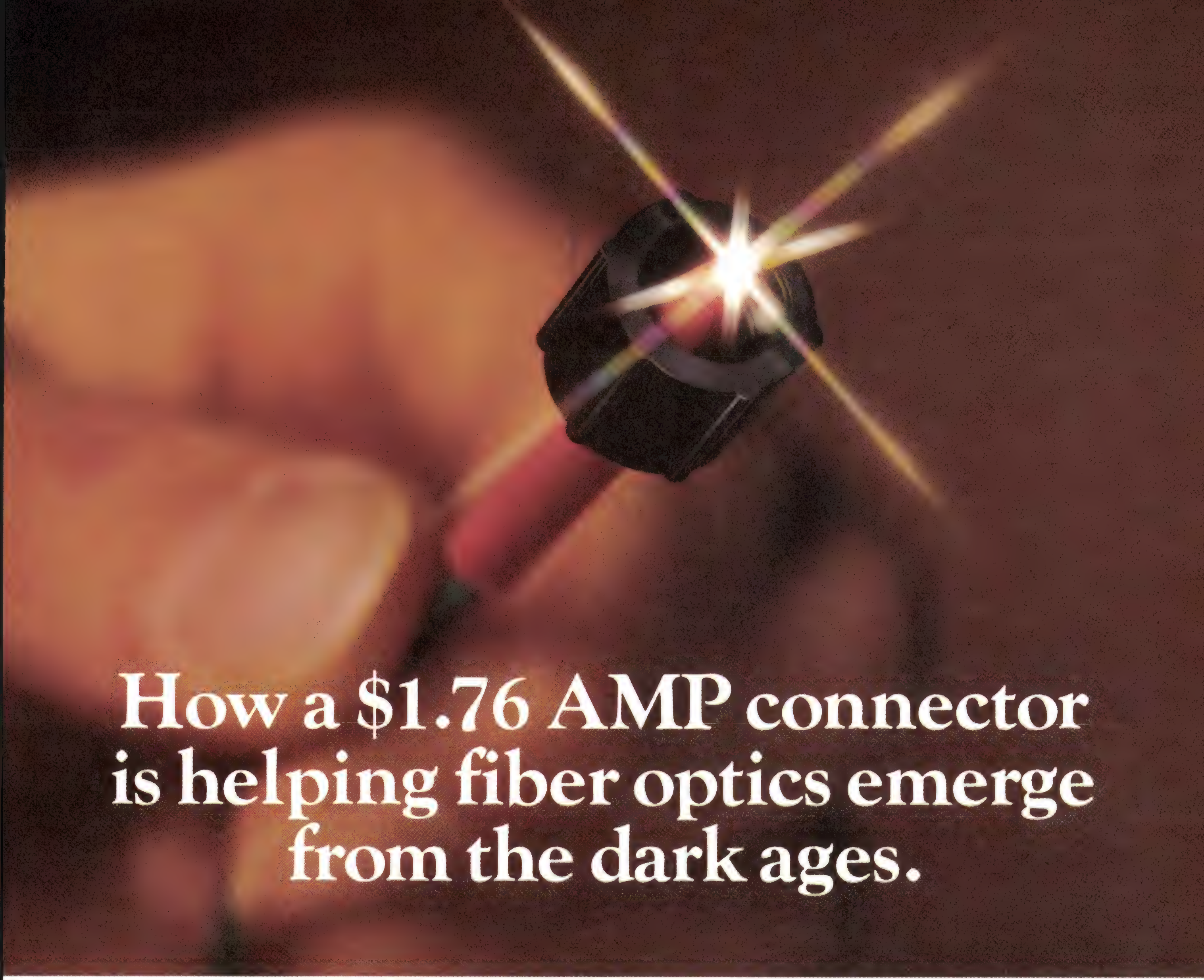
memory access controller, an interrupt control unit and a clock generator. All circuits, including the CPUs, will be introduced this year.

The floating-point processor, for high-speed operations on single and double-precision operands, will contain eight 32-bit data registers and a 32-bit floating-point status register. It will execute 14 instructions, including multiply, divide and conversion from one precision type to another. When used with the 16032, the floating-point processor will operate as a slave; however, with any other bus-compatible CPU that cannot use it as a slave, the floating-point processor will operate as a peripheral.

Another circuit is the memory-management unit. Capable of expanding the memory addressing range to 32 Mbytes, the MMU will fit between the CPU and memory, driven directly by the CPU bus. Providing four major functions to support the CPU, the MMU will handle memory mapping (converting virtual addresses to physical or real addresses) and memory protection, (four levels of protection provided for each page). It will support software debugging in a virtual machine environment and hardware debugging in an in-circuit emulation environment. Its automatic associative-memory cache will help with address translation.

Since the MMU can perform software debugging in a virtual environment, both virtual memory and virtual machines can be supported.■■

How useful?	Circle No.
Immediate design application	550
Within the next year	551
Not applicable	552



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CIRCLE NUMBER 39

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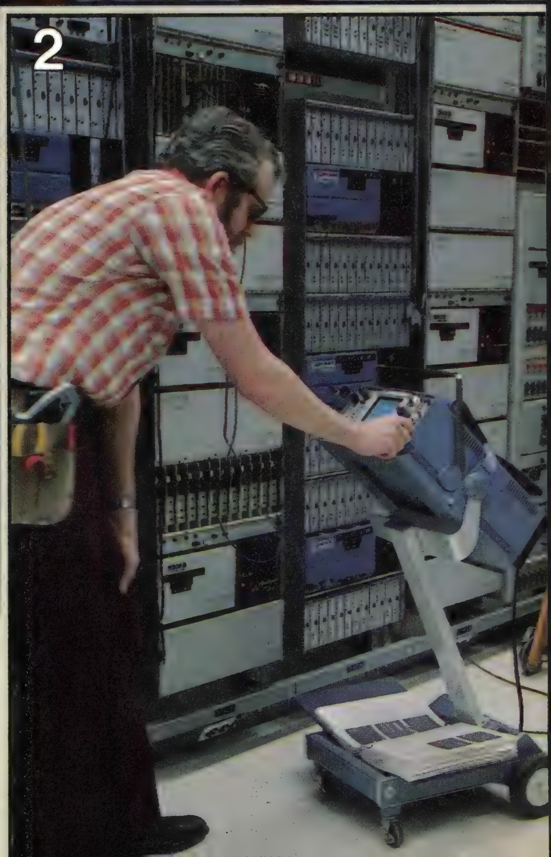
*Quantity price for two connector halves and splice bushing

Tektronix

1

2



Tektronix offers 15 storage scopes and the widest selection of storage modes. Here is how just a few of those scopes are being used today.

1 The FAST storage mode of the 7834 being used to capture high speed laser pulses.

2 The extremely bright display provided by the 466 in variable persistence mode makes it easy to view low rep rate switching performance.

3 The TM 500 with an SC 503 bistable storage plug-in being used for audio maintenance.

4 The highly portable 214 at work in system troubleshooting.

5 The long view time provided by bistable storage in the 5111 is useful for the study of pain threshold data.

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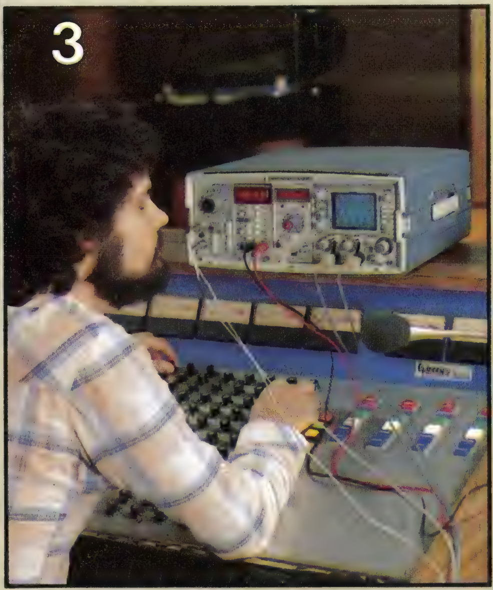

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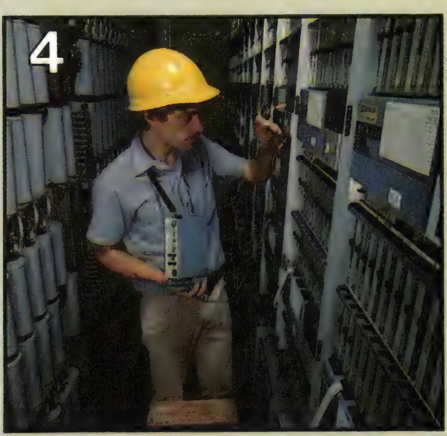

5

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Moving from 20-kHz to over 200-kHz operation puts more punch in switcher performance

This article on switching regulator topologies is the first in a series on high-frequency switchers. Future articles will deal with the construction and selection of high-frequency components and circuit design.

Armed with better switching transistors, generally improved components and the right circuit topologies, switched-mode converters—hitherto a fixture at 20 kHz—can now take advantage of performance increases by operating not only above 200 kHz, but into the MHz region.

For medium power (>100 W) offline switching supplies using bipolar switches, the optimum frequency is around 200 kHz. Low-voltage dc supplies can operate even higher—in the 300 to 600 kHz range. If power MOSFETs replace bipolars, switching frequencies can move up to the MHz range, at least for low-power designs.

Doubling or tripling the 20-kHz frequency gains little since cost, volume, weight and bandwidth improve slowly as frequency increases. Significant advances appear when the switching frequency is increased by an order of magnitude. At high frequency, not only is the size of magnetic components reduced, but it becomes possible to use materials and components that offer lower cost and improved performance.

Below 100 W, there are few reasons to operate around 200 kHz—components are not much smaller or cheaper. In fact, the lower the power, the easier it is to take advantage of air-core magnetics and power MOSFETs to operate in the low-MHz region. Above 1 kW, bipolar switches must be used, but operating frequencies must move down towards 100 kHz to match the speed of bipolar devices.

Topology tells the tale

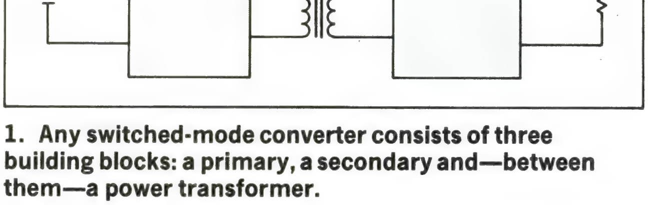
Circuit topology plays a major role in determining power-supply performance at 200 kHz and above. While the common 20-kHz topologies—parallel, half-bridge, full bridge, etc.—could be used at 200 kHz, performance would be far from optimum.

Any converter can be viewed as having a primary and secondary topology, connected by a transformer (Fig. 1). While the main problem is to design a power transformer to operate at 200 kHz, each of the converter's three main elements—primary, secondary and transformer—must be considered in relation to the other two. Selecting an improper primary switch or output-rectifier connection can render the transformer impractical at 200 kHz.

Looking first at primary topologies, the designer must choose between switched-mode (modified square waves) and resonant converters. If the former is selected, the designer may choose from three types of topologies: voltage-fed, current-fed with non-overlapping switch conduction, or current-fed with overlapping conduction. Table 1 gives the pros and cons for each option.

Although many resonant circuits are available, they have yet to be used widely at high frequencies, so there isn't much direct experience with them. Theoretically, however, resonant converters should work well, and if it becomes possible to operate current-fed switched-mode circuits in a resonant mode by adding a resonating capacitor, many new resonant-converter topologies will become available. Another possibility is that some SCR inverter circuits can be used as high-frequency resonant inverters, with power MOSFETs replacing SCRs as the switches.

Examples of good and bad choices for high-frequency switched-mode topologies are shown in Fig. 2a and b. Fig. 2a is a current-fed circuit, Fig. 2b a common voltage-fed bridge quasisquare-wave converter. From the comparison of the two types given in Table 2, two



1. Any switched-mode converter consists of three building blocks: a primary, a secondary and—between them—a power transformer.

Rudolf Severns, Power MOSFET Applications Manager, Intersil, Inc., 10710 N. Tantau Ave., Cupertino, CA 95014.

Table 1. Regulator-topology tradeoffs

Advantages	Disadvantages
Voltage-fed-Converter	
1. Wide variety of circuits 2. Good output regulation at heavy loads 3. Well-understood circuits	1. Current spikes 2. Switch overlap (fatal) 3. Poor capacitive losses at low power 4. Poor output regulation at light loads 5. Poor EMI characteristics 6. High switch transition
Current-fed converter	
1. Wide variety of circuits 2. No current spikes 3. O.K. storage-time overlap 4. Good multiple-output regulation at all loads	1. Voltage spikes 2. Poor capacitive losses at low power 3. Moderate EMI characteristics 4. Moderate switch-transition stress
Resonant converter	
1. Low switching loss and stress 2. Low capacitive loss 3. Low EMI	1. Resonating capacitors required 2. Current or voltage increases due to Q multiplication 3. Fixed-frequency operation difficult 4. Increased circuit complexity

Table 2. Current-fed vs voltage-fed topologies

Advantages	Disadvantages
Single dc loop	
1. Well understood 2. Simple control circuits 3. For 20-kHz equivalent performance, a single low frequency pole may be used	1. Uncompensated moving capacitor ESR zero 2. Uncompensated variable load capacity 3. Load capacity may be much larger than IC filter requirements 4. Two-pole rolloff with peaking 5. Boost converters have right half-plane zero 6. Gain crossover limited to 10-15% of f_0 7. No inherent current limiting
Dc loop and switch peak current sense	
1. Inherent overcurrent protection 2. Inherent soft-start capability 3. Higher-gain crossover frequency 4. Right half-plane zero compensation 5. Single-pole rolloff 6. Inherent current sharing for parallel modules	1. More complex control circuit 2. Switch current-sensor required 3. No compensation for moving ESR zero 4. No compensation for varying load capacity
Dc loop and inductor voltage sense	
1. Higher-gain crossover frequency 2. Right half-plane zero compensation 3. Compensation for variable load capacitance 4. Moving ESR-zero compensation 5. Single-pole rolloff	1. Complex control circuit 2. Choke voltage sensor required 3. No inherent current limiting
Feed forward	
1. Very simple in dc loop systems 2. Compensates for loop-gain variation with duty cycle 3. Improved line-transient response	1. Difficult to apply to multiloop systems 2. Not adequate as regulation loop by itself

things become clear: There are advantages to using circuits not widely used at 20 kHz, and current-fed converters are more suitable than voltage-fed at high frequencies.

But neither topology nor switching frequency is the whole story—especially when the choice of a power switch can affect the topology.

Where power switches fit in

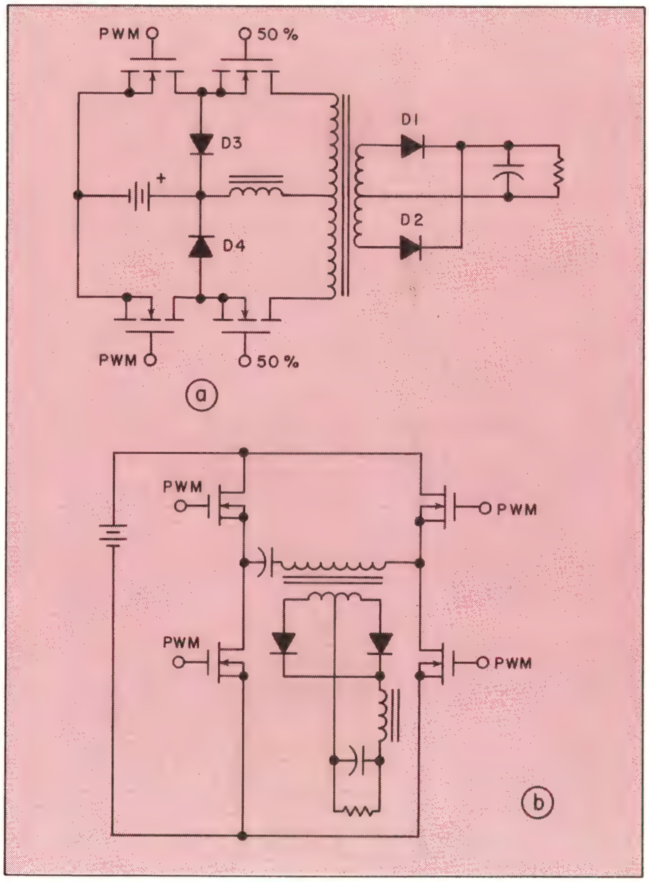
Power MOSFETs, which can make transitions in a few nanoseconds, are very appropriate as high-frequency switches. But if they are selected, the topology used can have an important effect on conduction losses.

Fig. 3 shows two converters that use power MOS devices: a conventional half-bridge quasisquare-wave converter (Fig. 3a), and an unmodulated half-bridge, preceded by a boost regulator (Fig. 3b). Assumed operating conditions for both circuits are also given. Note that the power losses in Fig. 3b are much lower than in Fig. 3a. The circuit in 3b requires three transistors to 3a's two, but because the cost of MOSFETs depends heavily on the reciprocal of r_{ds}, the MOSFET on-resistance, the three devices actually could be much less expensive than the two.

While the examples in Fig. 3 are simple, valid conclusions can be reached when a variety of different topologies are compared. For example, boost-derived converters generally provide lower MOSFET conduction losses than buck-derived, current-fed converters.

Two of the many possible boost circuits are shown in Fig. 4. Overlapping conduction is used in Fig. 4a while Fig. 4b has a secondary shunt switch. While both —indeed all—boost circuits have advantages, beware of their drawbacks:

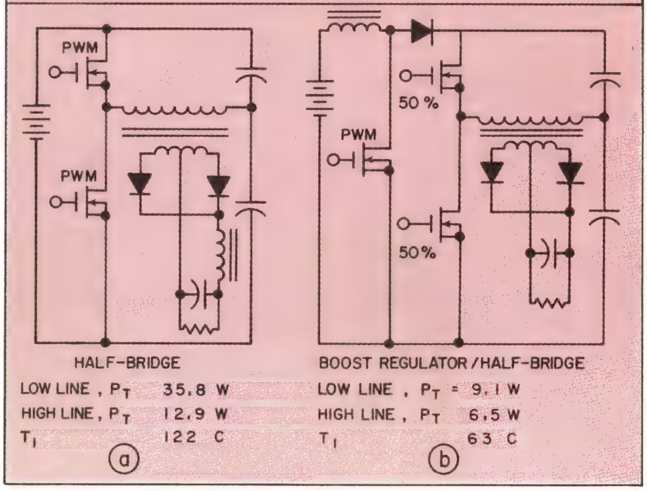
- The control-loop transfer function has a right-half-plane zero, which is difficult to compensate with single-loop feedback. But multiple ac and dc loops will overcome the problem.
- A boost converter's output ripple current is discontinuous, but the input current is continuous. The result? Large output ripple current. Because low-voltage (< 50 V), high-current film capacitors are not readily available, designers have to pay a penalty in component size for low-voltage outputs.
- Where overlapping conduction is used in the primary, a large voltage spike can be generated because of the interruption of the primary-to-secondary leakage inductance current. But spiking is significantly reduced by placing a shunt switch in the secondary.



2. Not all converter circuit topologies work well in the high-frequency domain. Above 100 kHz, a current-fed design (a) is a better choice than a voltage-fed bridge quasisquare-wave converter (b). All the reasons, pro and con, are given in Table 2.

Assumed conditions

P_0 = 200 W
η = 80% without switch losses
V_{dc} = 200 to 375 V
T_a = 50 C
R_{DS} = 2.5 Ω at 25 C
Filter inductor is large
BV_{DSS} = 450 to 500 V
$\theta_{j\text{-}a}$ = 4 C/W (TO-3 case and heat sink)
r_{DS} tempco 0.6%/°C



3. Transistor switches play a key role in determining which type of topology works best at high frequency. Power MOSFETs are the switches in both a half-wave quasisquare-wave converter (a) and an unmodulated half-bridge preceded by a boost regulator (b).

Table 3. Fixed-frequency control-system options

Current-fed	Voltage-fed
1. Even with fast-recovery diodes, the reverse recovery time of the output rectifiers is a significant portion of the operating cycle. Diode D_1 will be in forward conduction while D_2 is still recovering. This places a short circuit across the secondary, which is reflected into the primary. Because this circuit is current-fed, the only effect is to slightly increase the energy stored in L_1, thus preventing current spiking in the switches.	1. During the rectifier reverse-recovery time, a current spike is reflected into the primary switches. At 200 kHz, the transformer leakage inductance is made quite small by design, so there is very little impedance to limit the current spike. If Schottky-barrier diodes are used, the large diode capacitance will also cause primary current spikes.
2. With the full-wave rectifier shown, the output rectifier's reverse voltage will be twice the output voltage plus one diode drop (not including noise), regardless of the line voltage. The value of dv/dt is also low so that hot carrier diodes can be used above 5 V.	2. For a given output voltage, the diode reverse voltage is relatively high. For example, with a 5-V output and a 2:1 line excursion, the rectifier reverse voltage varies from 11.7 to 22.8 V. If the switch storage time reduces the maximum on-time to prevent overlap, then the reverse voltage is even higher. The higher reverse voltage also increases the dv/dt to which the rectifier is subjected.
3. At high frequencies, there is a greater tendency towards primary volt-second asymmetry, especially if bipolar switches are used. This can cause core-saturation current spikes in voltage-fed topologies. In this circuit, spiking is prevented by L_1 so that core saturation is relatively harmless. Current spikes due to reflected capacity and switch overlap are also suppressed.	3. There is no protection from core saturation, switch overlap or reflected winding-capacitance current spikes. In the case of bipolar switches, the need to prevent overlap due to storage time, allowing for manufacturing and temperature variations, can significantly reduce the pulse width's dynamic range. Core saturation can be reduced by inserting a series capacitor in the primary, but this capacitor must be carefully selected to prevent core saturation during fast-line or load slewing.
4. Because a single choke is common to all outputs, cross-regulation between the outputs for varying loads is relatively good.	4. Separate chokes are required on each output and for good regulation each choke must remain in continuous conduction. There is no compensation for the choke's resistive regulation effects. As a result, cross-regulation of multiple outputs is poor at 200 kHz.
5. Diodes D_3 and D_4 do not see a reverse potential at the end of their conduction cycle, so the reverse-recovery time of these devices is not critical.	

Now the secondary—rectifier—topology can be selected, along with the output transformer. Both the transformer's limitations and the primary topology requirements must be considered.

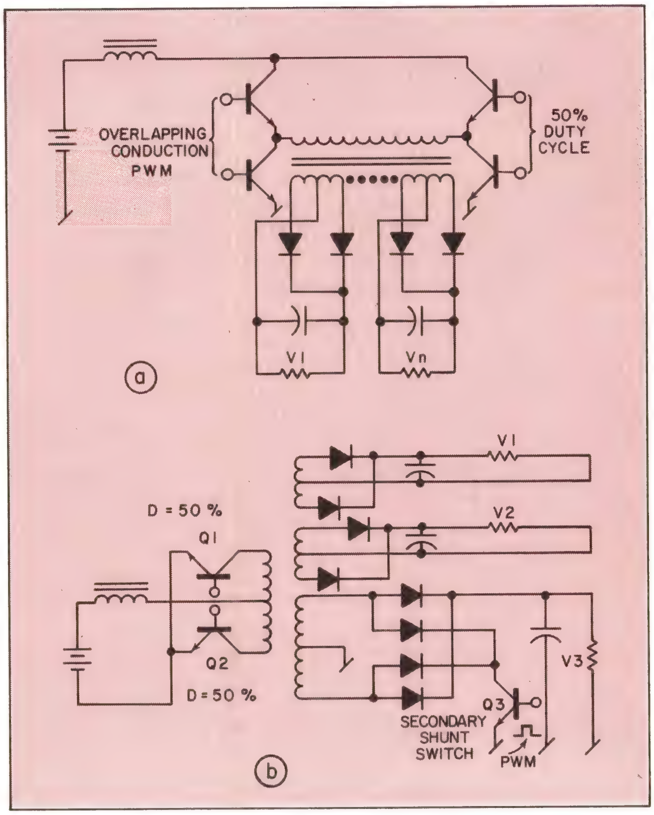
Output windings and rectifiers

Fig. 5 shows two rectifier connections, both for multiple outputs. In Fig. 5a, separate windings are used, while Fig. 5b represents an autotransformer connection.

If dc isolation between outputs is not required, Fig. 5b provides superior results because it gives better cross-regulation. A major cause of poor cross-regulation is the leakage inductance between the secondary windings—an effect that gets worse at higher frequencies. With an autotransformer, leakage inductance is minimized, and resistive compensation is provided for load variations.

If a high output voltage is required, there are two choices for the output winding-rectifier topology: multiple windings or voltage multipliers (Figs. 6a and b). Multiple windings pose problems for transformer construction because of the need for stacked, insulated windings. The insulation spacing depends on the voltage, not the operating frequency, and at 200 kHz good primary-to-secondary coupling with uniformly predictable winding voltages is difficult to obtain.

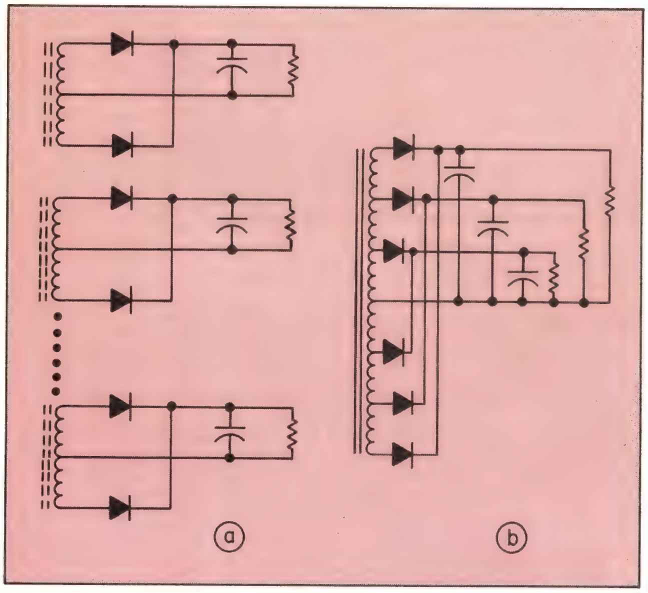
With a voltage multiplier, the transformer design is easier, but many capacitors are required. For-



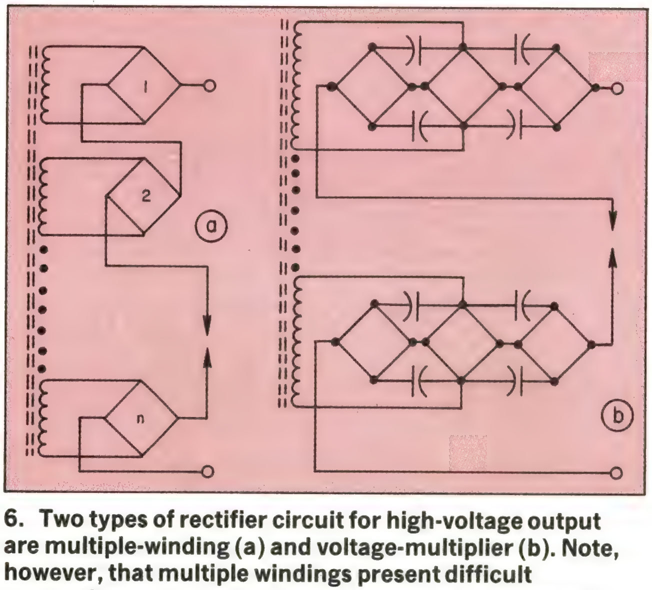
4. Of the possible high-frequency boost-derived circuits, (a) uses overlapping conduction, while (b) has a shunt switch in the secondary. A shunt switch limits primary voltage-spiking stemming from primary-secondary current interruption.

tunately, at 200 kHz the capacitors can be small. The most serious limitation for high-frequency multipliers is diode shunt capacity, but if the multiplication ratio is small (3 to 5) and the power levels reasonable (> 10 W), the problems are minimized.

For voltages in excess of 1 kV, multipliers greatly simplify magnetics design. However, the reflected capacitance from the high-voltage transformer secondary will be large. And even though the leakage inductance is increased, the primary switch currents are usually unacceptable in a voltage-fed topology—some form of current-fed circuit gives better performance. But a voltage multiplier will see wide, low-amplitude current pulses rather than short, high-amplitude current spikes. This serves to reduce losses and improve the output regulation.



5. For multiple-output voltages, either of these rectifier connections can be used. The separate windings (a) provide dc isolation, but if isolation is not required, an autotransformer circuit (b) is a better choice because of the good cross-regulation it provides.



6. Two types of rectifier circuit for high-voltage output are multiple-winding (a) and voltage-multiplier (b). Note, however, that multiple windings present difficult magnetics problems, while multipliers are hampered by diode capacity.

Just as the input and output topologies in a switched-made converter involve tradeoffs, so does the feedback, or control, scheme.

Control option pros and cons

Increasing the switching frequency from 20 to 200 kHz provides a similar increase in the feedback-loop gain crossover frequency. With the proper type of control loop and compensation, a gain crossover of 20 to 100 kHz is possible, and this is comparable to the usual series regulator.

There are four commonly used fixed-frequency control schemes for high-frequency converters, and their advantages and disadvantages are listed in Table 3. But the control problems encountered at 200 kHz are far different from those at 20 kHz. For example, at 20 kHz the output filter capacitor is usually picked for low equivalent series resistance (ESR); capacitance value is a secondary consideration. What's more, the filter capacitor is usually larger than the load capacity.

All this changes at 200 kHz: Film capacitors have an ESR about 100 times less than at 20 kHz, the filter capacitor is physically smaller, and the load capacity may very well be larger than the filter capacitor. Another difficulty is that the load capacity can be undefined or variable. These factors make it difficult to stabilize the feedback loop. To complicate matters further, if power modules are to be paralleled, each loop not only sees the capacity of the other modules, but the modules themselves can have variable values of capacitance.

With a boost-derived topology, there is a right half-plane zero in the control transfer function. And it is not easily compensated with a simple dc averaging control loop. Much better performance results if a combination of ac and dc loops is used, and in general multiple-loop control schemes are recommended above 100 kHz.

At 200 kHz, stray capacity is likely to cause problems. Since stray capacity is proportionately larger than at 20 kHz, the likelihood of subharmonic instabilities from capacitive feedthrough at the ripple frequency increases. Careful layout and good bypassing will combat this effect.

In some types of pulse-width controller circuits, time delays through the digital elements (especially CMOS) can be large enough to cause significant phase shift. In a 200-kHz converter, delay times through the controller should be held below 5% of the half-period, or about 100 ns.■■

How useful?	**Circle No.**
Immediate design application	**541**
Within the next year	**542**
Not applicable	**543**

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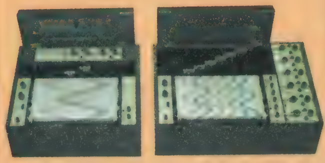

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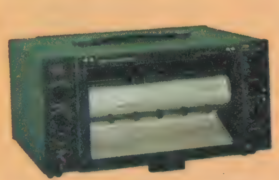

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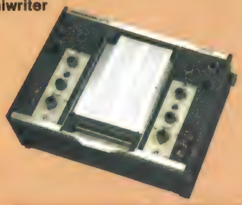

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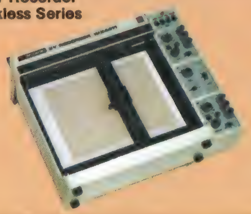

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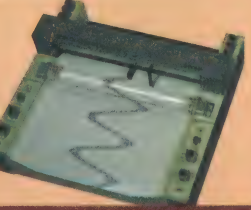

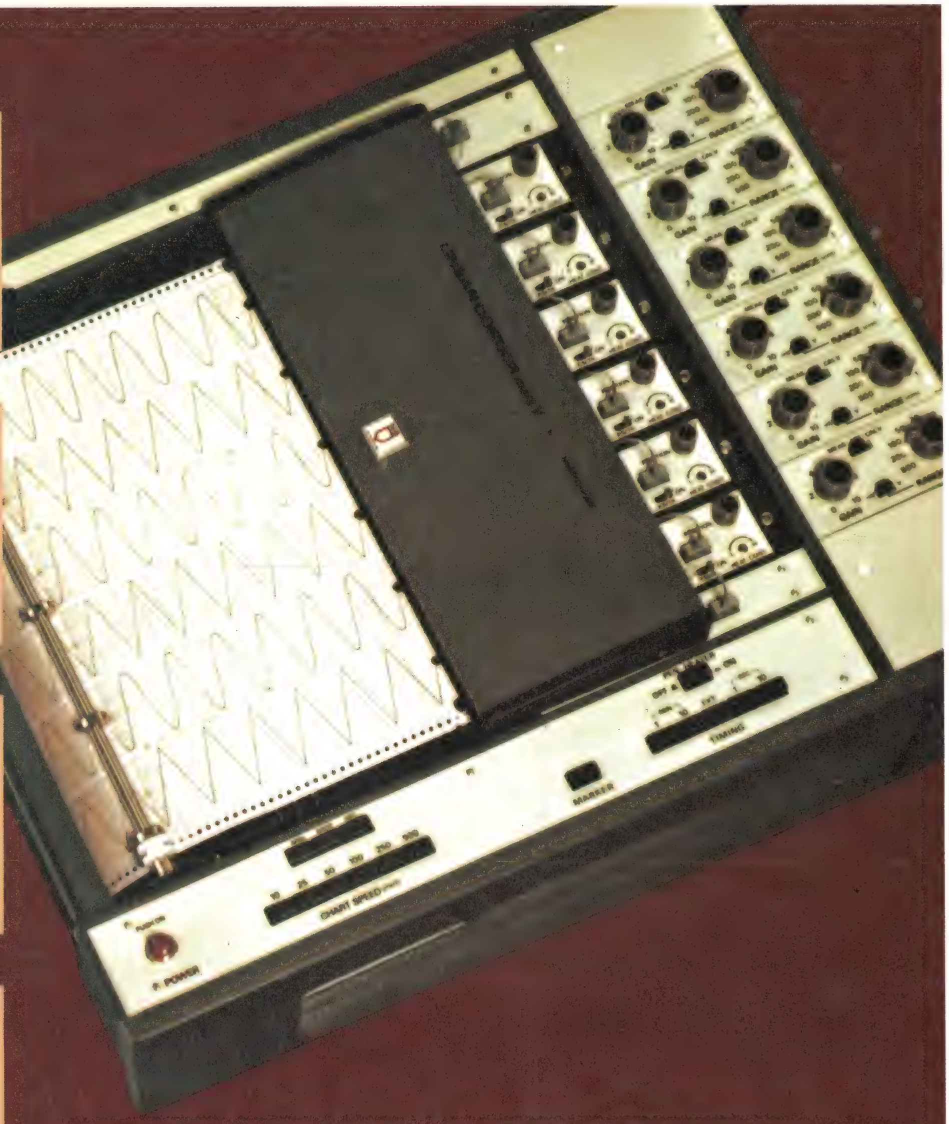

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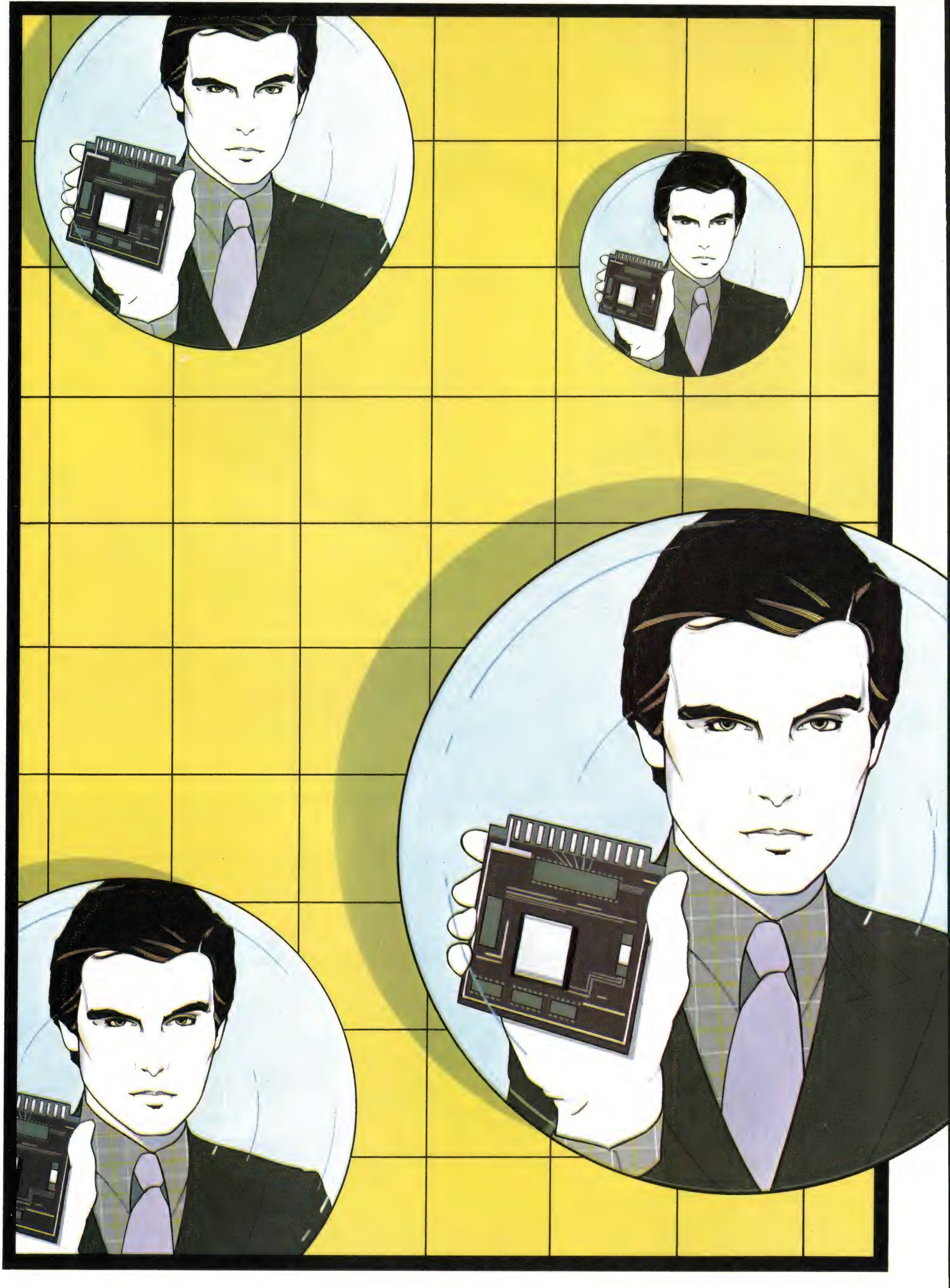

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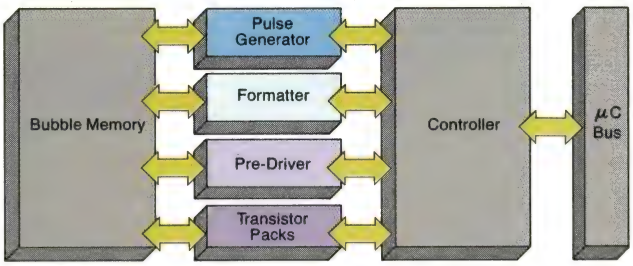

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CIRCLE NUMBER 42

Dual-μC design adds memory, processing and software control without adding chips

While a single-chip microcomputer adds intelligence and labor-saving conveniences to a low-cost instrument, the complex functions to be performed often demand more I/O and memory than one chip can provide. A common solution is to add as many external components as are needed—which could raise both chip count and cost significantly. However, there is a way to add memory and I/O without the usual components—use a second single-chip μC, which will also provide more computing power and hence more software control.

To see how effective this approach can be, examine a design for a low-cost instrument to be used for automatically measuring the chemical concentrations of a liquid solution. The functions it must perform are complex enough: For one thing, it must provide a direct readout of detected concentrations and perform automatic calibration based on standards of known concentrations and operator input. Not only that, but displayed results must be calculated from input data using an algorithm requiring about 15 equations, many involving logarithmic and exponential functions.

The single-chip solution

In addition, samples are to be tested using an ion-selective electrode as a sensor, placed into the sample solution. This requires a/d conversion with a resolution of 15 bits plus sign. Results are to be relayed to the operator via a LED display while operator input is accepted via a front-panel keypad.

In terms of cost, a single-chip μC would be the most attractive solution. Problem is, there simply isn't a device available that could supply all the required ROM, RAM and I/O without enlisting the support of many external chips, commonly configured in bus architecture.

How many? In this case, a total of 14 chips (Fig. 1). But high chip count is only one of many drawbacks. For one thing, such a configuration needs a two-chip set: the LD120 analog processor, which requires many discrete components not even shown in Fig. 1, and the LD121 synchronous processor for a/d conversion. The synchronous processor must perform some of the processing that could not be carried out by the microcomputer.

But there is an even bigger drawback. To reduce parts count for this arrangement, the μC would have to be responsible for scanning the instrument's matrix keypad and eight-segment display in a polled mode. This, in turn, would increase the design's software load. What's more, timing conflicts would have to be resolved among a/d control and readout, display/keypad, scanning and mathematical computation without the μC.

Double up and save

On the other hand, the two-μC solution depicted in Fig. 2 cuts chip count in half by providing 6080 bytes of ROM, 192 bytes of RAM, and the I/O ports (PIAs) incorporated in both. In addition, the increased computing power provided by the second μC allows software control of the analog processor used for a/d conversion. This means the synchronous processor and divide-by-four of the first design can be replaced by an LF13300 analog processor.

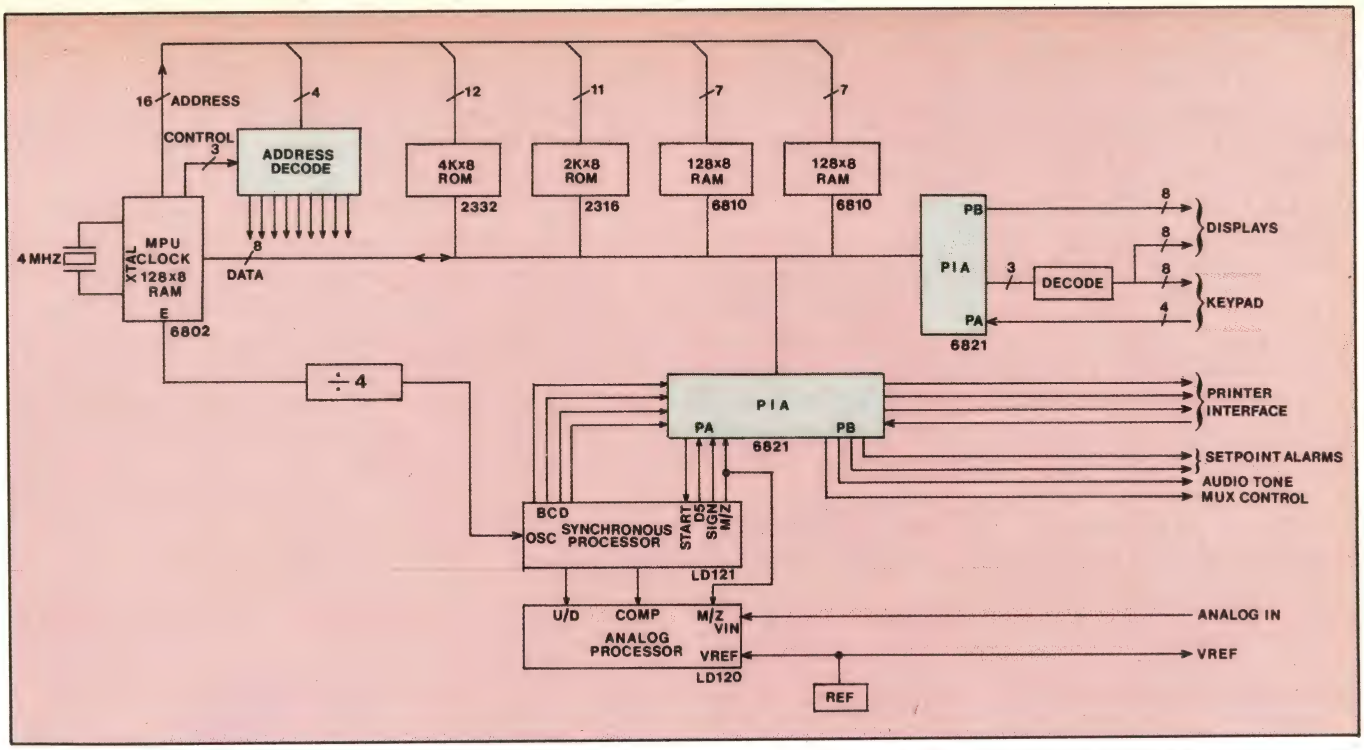
With this added processing capability, the real-time task of controlling the analog processor is assigned to one microcomputer while the other handles all remaining real-time tasks: display refresh, keypad scan, printer interface, setpoint alarms, audio tone and sampling rate.

To keep the software design simple, the μCs are programmed to be master and slave, the master 3872 using the slave 3870 as a smart peripheral, sending it commands and data. The slave returns data on command.

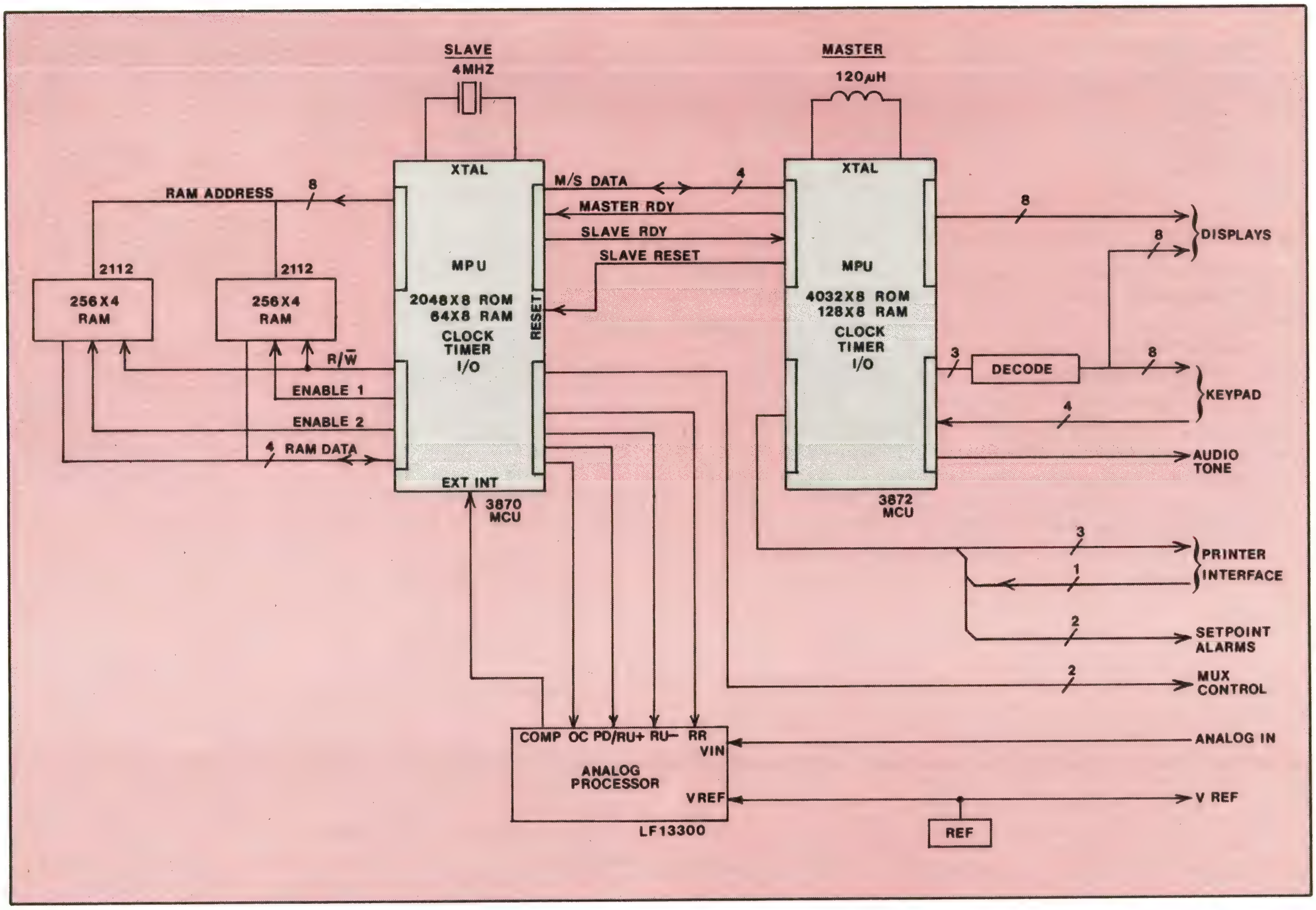
Each master-slave exchange begins with a command from the master, followed by a data transfer if required by the command. After each exchange, the slave goes dormant to await the next command. In this way, the master controls the direction and use of the interface.

The master and slave communicate commands and data over a 4-bit bidirectional data bus (M/S DATA). All transfers on this bus are synchronized under software control by MASTER RDY and SLAVE RDY (Fig.

C.N. Carter, Senior Project Engineer, and **J.J. Kalinowski,** Supervisor, Instrument Development, Technical Staffs Div., Corning Glass Works, Corning, NY 14830.



1. Employing a single microcomputer in a commonly used bus-organized architecture requires 14 chips and a program susceptible to timing conflicts. Some chips are needed for adding memory and I/O components like the address-decode function, which is needed to access not only the added program memory but also the PIAs required to support the added I/O. Other shortcomings of this approach lead to the need for even more parts.



2. This multiprocessor approach not only cuts the chip count of the bus-organized architecture, it eliminates the bus and provides greater and more widely dispersed processing power. One microcomputer performs operator interface, and one specializes in floating-point and real-time processing.

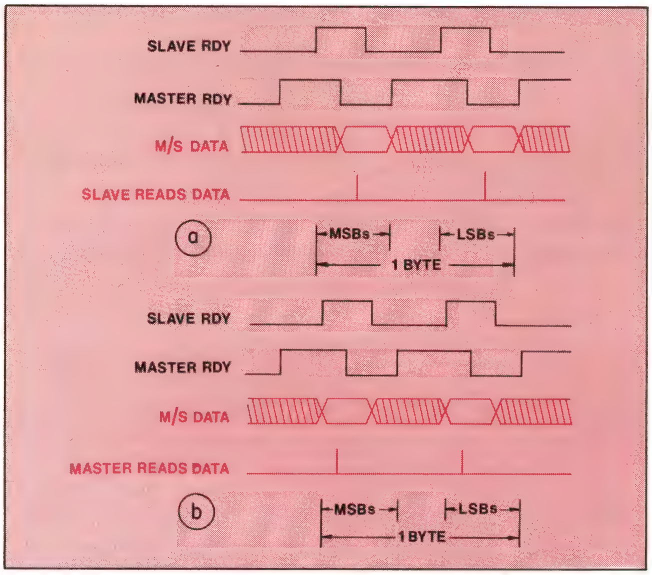
3a). To abort an operation, the master resets the slave to its initial power-on state by asserting SLAVE RESET. With this interface, 8-bit bytes can be transferred in two operations. In addition, the interface can be implemented using only one I/O port on each microcomputer. (A similar sequence for slave-to-master transfers is given in Fig. 3b.)

Commands to the slave call for either some action or data transfer. Action commands are single-byte command codes that direct the slave to perform tasks, such as an a/d conversion or a calculation based on voltage readings and parameters stored in the slave's memory. Data-transfer command sequences begin with the transfer of a single-byte command code that identifies a parameter in the slave's memory and the transfer direction.

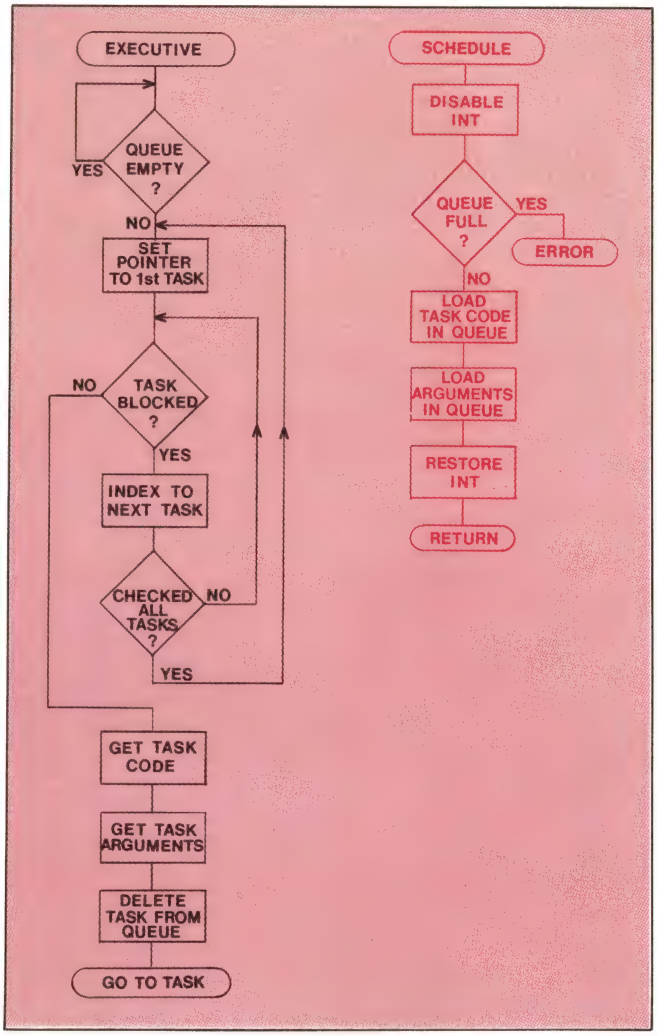
When the slave receives a data-transfer command, it enters a routine that transfers a fixed number of bytes between the identified memory locations and the master. Commands of this type are all the master needs to establish the parameters of a governing equation and direct the slave to measure a sensor output, then convert it into a displayed quantity.

There are hurdles to overcome with this design. For example, μCs don't always provide enough RAM for data storage, which can be a real problem if the data and address buses are not provided for memory expansion. At the same time, however, it may be desirable to select a microcomputer that does not provide an expansion facility—the 3872—to obtain some other feature, such as the 3872's large ROM.

One solution to this RAM problem is shown in Fig. 2. Two RAMs, each 256 × 4, are interfaced via two I/O ports of the 3870, and accessed by cycling the address, data and control lines in the manner specified by the memory manufacturer. Using a 4-bit data



3. In master-to-slave communications (a), the slave waits for the MASTER RDY line to go high before raising its SLAVE RDY line to high. Once it detects SLAVE RDY, the master sends out 4 bits of data and drops its own MASTER RDY. The slave reads-in the bits, then drops its own SLAVE RDY signal to indicate that the data were received. Since 4 bits are transferred, each byte requires two sequences. In slave-to-master communications (b), the master commands a transfer from the slave, whose execution of the command results in the timing shown. Slave-to-master communication works like master-to-slave except that as the slave raises its SLAVE RDY line, it supplies data for the master to read.



4. As the flow diagram shows, every time a task is executed, the executive program passes arguments—variables, commands, etc.—to the task software from the schedule program. Because the executive saves the contents of microcomputer registers, the task software is free to use them without doing this housekeeping function itself. When the task is completed, it performs a return to the executive program, which initiates the next task to be performed.

structure makes it possible to interface the equivalent of 256 bytes of RAM with no additional hardware.

Read and write subroutines access the outboard RAM, transferring one 8-bit byte between the μC and RAMs. The low-order four bits are stored in one memory, and the high-order four in the other. This way a complete byte transfer takes but one access to the address port. To maintain system performance, frequently accessed variables are stored in the internal RAM. If a variable will be accessed several times during an operation, it is first transferred to a temporary location in internal RAM for the duration of the operation.

Another design complexity is the partitioning of tasks between microcomputers. The following guidelines should simplify matters:

- Minimize master-slave transfers.
- Keep similar routines in the same μC, especially if they can share common subroutines.
- Put routines in the processor that has the required I/O.
- Do not overburden either processor with real-time tasks.

In this design, tasks are partitioned so that all equations relating sensor outputs to displayed quantities are evaluated in the slave. Since these equations require a floating-point-arithmetic package, it helps to interface the a/d to the slave since the a/d processing also requires such a package. Moreover, all other floating-point calculations are done in the slave.

Because the calculations require memory to store calibration results and temporary values, it is important that the RAM be interfaced to the slave as well. To avoid timing conflicts that might cause a/d errors, the a/d routine is the only real-time task in the slave.

Accepting user inputs and commands, the master directs all instrument functions, communicating with the instrument operator via multiplexed displays and a scanned-matrix keypad. For this reason, the master contains all tasks required to parse operator inputs, execute commands, format displays and control instrument sequences. It is also convenient for the master to control the printer interface, setpoint alarms and audio tone since these are related to displayed data.

For both μCs, one way to make program execution more efficient is to use an executive program. It allocates processor resources and simplifies software design in any real-time environment—even in μCs. A simple executive that executes tasks from a queue on a first-in-first-out priority is outlined in Fig. 4. The priority can be modified by a flag that prevents a task from being activated until some external event, such as a real-time clock interrupt, clears the flag. Tasks can be scheduled from any background or interrupt level, but in either case are executed at the background level.

What's more, the executive makes the system more responsive to interrupts by allowing them to queue time-consuming processing for background execution. Tasks that must check noninterrupt-driven I/O flags can periodically reschedule themselves.

However, the executive cannot do all the time saving. While it can simplify the software designer's job by allocating system resources, the simple priority algorithm as well as the system's need to be responsive to interrupt-scheduled tasks compel the system designer himself to keep task executions short. Subdivide long tasks, if necessary.

Get the most out of the design

To reap the benefits of multiple microcomputer design while minimizing the drawbacks, use a general-purpose development system capable of supporting just about any processor that becomes available. This approach not only minimizes development effort, it even removes the development system as a factor in selecting the target processor.

The system used to develop Corning's pH/Ion Meter is a PDP-11, with standard peripherals and software for almost all commercially available micros. Also used is a simple debug system/emulator with integral monitor specific to the target processors, the 3870 and 3872 μCs. The required software includes a cross-assembler, an editor, a program to down-load object code to the debug system, and a program to format paper tape for an EPROM programmer. All hardware and software specific to the target processor(s) can be acquired for a small fraction of the total capital investment.

Since all μCs must be emulated before being committed to vendor masks, all coding and debugging for the 3872 slave are completed and committed to an EPROM-based emulator board before the master μC is coded.

Code for the master micro is then loaded into a second emulator board, thus allowing both emulators to be used in preproduction prototypes for field testing. Flow charts generated for all processors detail all functions from the point of view of an observer within the microcomputer.

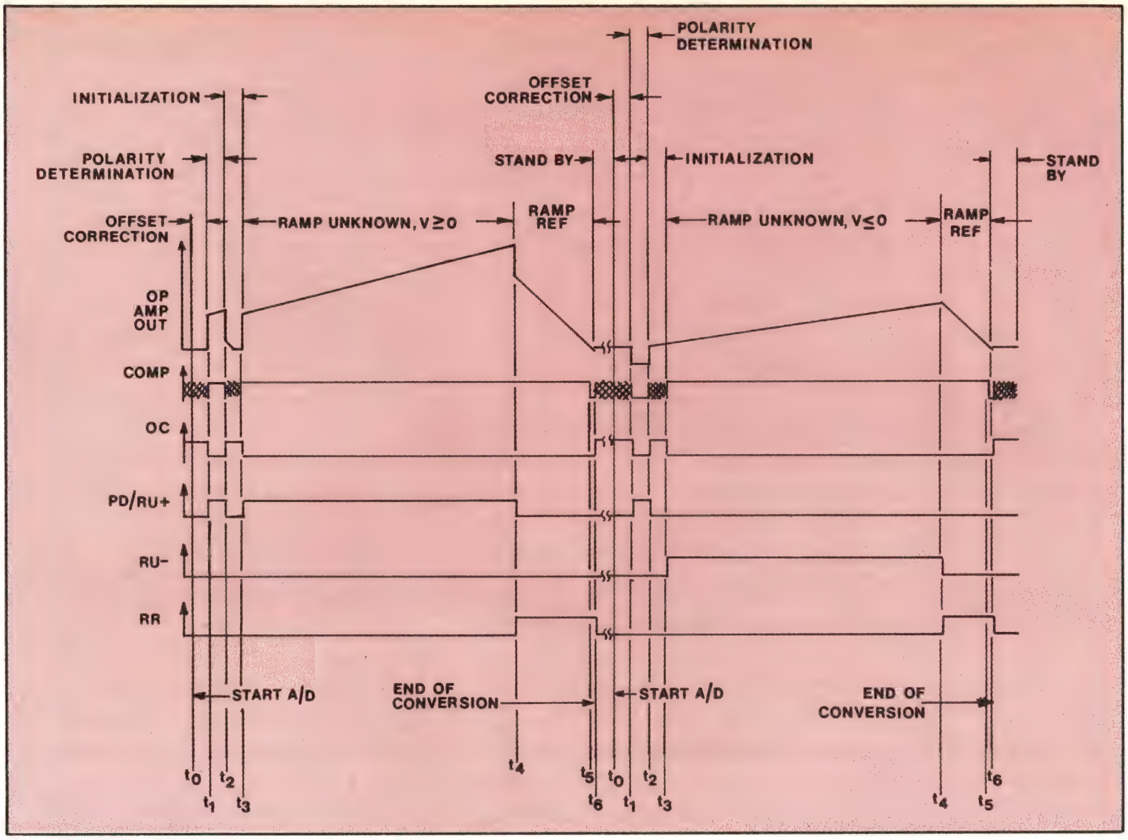
Both the master-slave interface and the slave-analog interface can be debugged effectively with a logic analyzer.

Control a/d with software

In addition, note that most single-chip μCs contain programmable timers that can be used to measure time intervals and pulse widths, two functions that make it simple to control the analog processor of the dual-slope a/d converter with software.

Fig. 2. shows the connection of an LF13300 to a 3870. Four bits of an I/O port generate the control signals: Offset Correct (OC), Polarity Detect/Ramp Positive Unknown (PD/RU+), Ramp Negative Unknown (RU−), and Ramp Reference (RR). The comparator (COMP) output drives the 3870's external interrupt input.

The rest state of the converter is offset correction



5. The timing diagram for the LF13300 analog processor shows the signal states of lines (running from the processor to the 8870 microcomputer) for both a positive and a negative analog input signal over two complete conversion cycles.

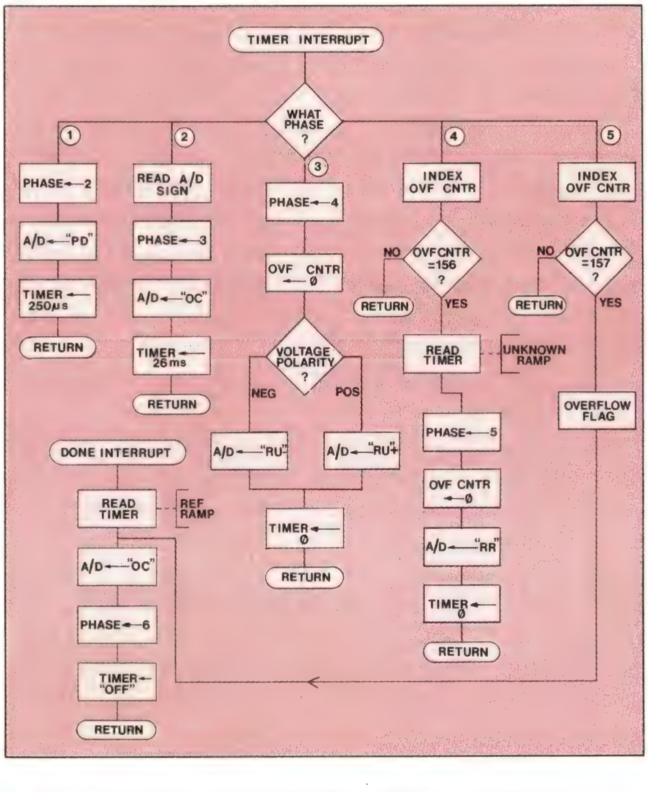
(Fig. 5). To start a conversion, the main program code sets the phase of the interrupt code to 1 and sets the interval timer for 26 ms, the duration of the first offset correction phase (T_0 to T_1). During conversion, the main program code continues background processing.

At the end of the first time interval, control briefly passes to the timer-interrupt service routine (Fig. 6). Phase 2, polarity determination, is then initiated for 250 μs. When this phase ends, the interrupt service routine reads the comparator output and remembers the polarity of the unknown voltage. Phase 3, another 26-ms offset correction, resets the integrator.

During phase 4, the unknown voltage is integrated for roughly 100 ms. Either PD/RU+ or RU− is tapped to be integration control, depending on the polarity of the unknown. The time interval for phase 4 is resolved to one part in over 40,000 by counting overflow interrupts from the 8-bit time register. The phase ends after 156 overflows.

Remaining counts in the timer register are combined with the overflow counter to form a 16-bit number. A correction factor, for the elapsed software time between reading the counter and reversing the integration, is added to determine the exact integration time for the unknown.

During phase 5, a reference voltage of opposite sign is applied to the integrator. In addition, the time required for the integrator to return to baseline is measured, using a mode that allows the timer to run



6. Program execution (analog-to-digital conversion) begins in phase 1 (not shown), then moves sequentially through these five subroutines, phases 2 through 6. Subroutine exits are directed by the time-out of a specific timer for the particular phase.

7. One product of multiprocessor design is the Corning 135 pH/Ion Meter. Compact and low-cost, it takes advantage of a dual-μC design approach to offer many attractive operator features and conveniences, such as an adaptive digital filter to stabilize displayed results.

only if the 3870's external interrupt input is high. As in phase 4, the time is resolved to one part in over 40,000 by counting overflow interrupts.

Finally, the timer is halted on the falling edge of the comparator output, and a completion interrupt routine executed. The timer register is again combined with the overflow counter to form a 16-bit number, and another correction factor is added for elapsed software time between starting the reference integration and starting the timer.

The unknown voltage is determined by multiplying the reference voltage by the ratio of the reference's integration time to the unknown's integration time. If 157 overflows are counted during phase 5, a/d overflow is assumed and the conversion stopped. To indicate completion to the main program, the completion routine sets the phase number at six.

The master/slave multiprocessor design approach works, as evidenced by Corning's 35 pH/Ion Meter (Fig. 7). All requirements have been fulfilled, including production cost. ■■

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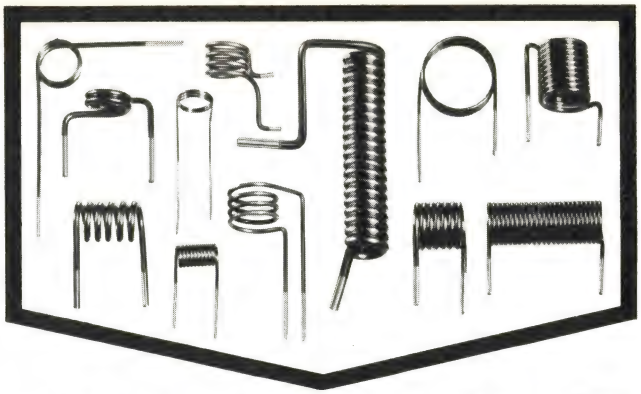
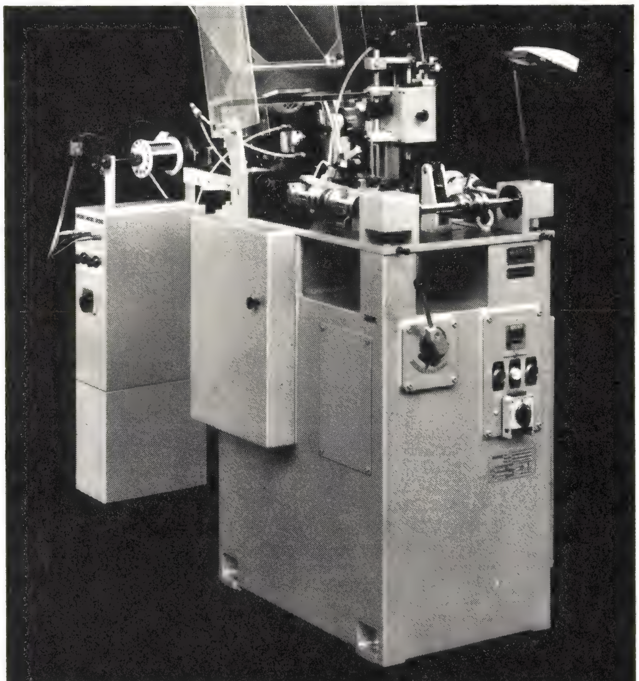
Aldridge, D., "Analog-to-Digital Conversion Techniques with the M6800 Microprocessor System," Motorola Application Note AN-757, 1975.

Kalinowski, J.J., "Ion Measurements Come of Age with an Assist from Microcomputer Technology in Electrochemical Assay," *Industrial Research Development, February, 1979.*

How useful?	**Circle No.**
Immediate design application	547
Within the next year	548
Not applicable	549





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ted with thick-film technology, the chip
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chip is designed (Fig. 1a) so that the
extend approximately 0.01 in. (0.25 mm)
op and bottom. Because of this small ex-
wiring trace—set between the two traces
the resistor is connected—may be bridged
sistor chip without danger of shorting. The
be mounted with its resistive element up or
th little or no effect on performance.

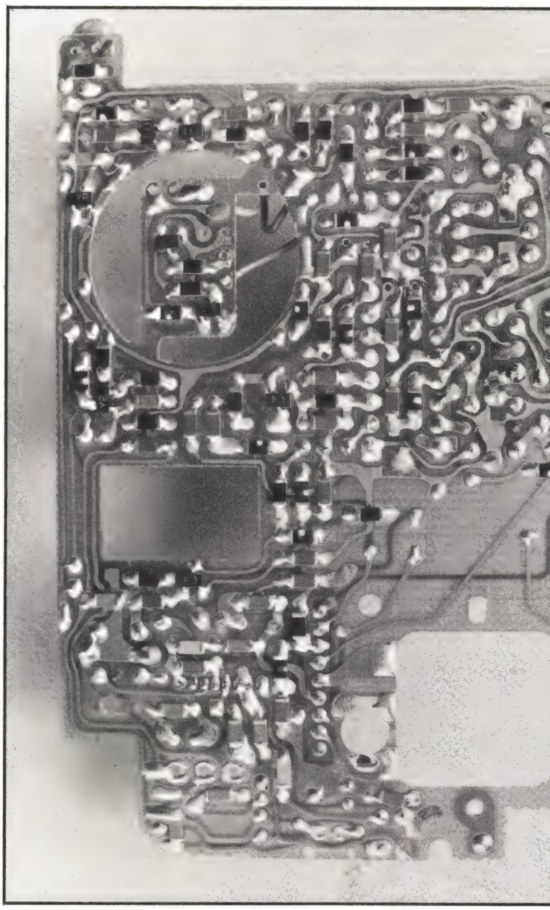
rast, a conventional chip resistor (Fig. 1b)
soldered directly to a PC board. The chip's
do not extend around the ends of the device,
rminations cannot withstand wave-soldering
ures.

CR-18 chips are built on a pre-scored sheet
a, which serves as a substrate. The resistive
made of ruthenium oxide, deposited so that
s the silver-palladium electrodes (Fig. 2).
top portion of the electrodes, the resistive
nd a protective glass coating are formed, the
he chips are separated where the electrode
to adjacent chips.

vs of chips, now joined only along the sides,
for the next step—the screening-on of
electrodes around the exposed ends. Next the r
separated, and each chip is sandblasted to tr
proper resistance. Trimming removes a smal
the glass coating and the resistive film with
grading the chip's characteristics.

Heat dissipation is excellent because of t
thermal conductivity of the alumina subst
nickel barrier layer added to the electrode pro
silver-palladium during soldering, and a so
outer layer facilitates soldering.

With its small size, the chip encourages ex
high-density mounting. Moreover, it can be
practically anywhere on the PC-board surfac
soldering provides a solid connection, and the
of the lead wires frequently used with conv



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Before the chips can be soldered to the board, they must be glued to the board surface with an epoxy adhesive. After the epoxy has hardened, it must withstand solder temperatures of up to 250 C. (A quick-drying epoxy with a long potting life and high viscosity, such as Epo-Tek H70, works best.) The mixture of epoxy resin and catalyst can be tailored so that potting life and drying time match assembly-line flow.

Automatic attachment—a two-way choice

The user can choose between two methods for attaching the chips automatically. With one method, hundreds of chips are loaded into magazines and mounted simultaneously, using specially designed equipment. In the other method, the chips are mounted on tape reels, and attached using an air-tweezer technique. Although the magazine method is considerably faster, the flexibility of the air-tweezer technique makes it more cost-effective for board runs at low volumes and for applications where the setup must be changed frequently.

With the magazine technique, the chip components are positioned according to a layout grid. Through a stainless-steel screen, a tiny drop of epoxy is applied automatically where each chip is to be attached to the board. To prevent the epoxy from flowing over the copper trace, a small rectangular spot of glue is applied at a right angle to the trace.

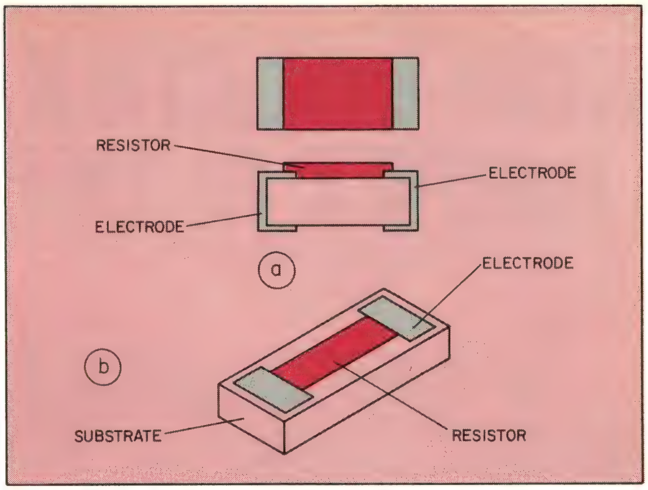
The chips are loaded into rectangular plastic magazines. Each magazine can contain up to 200 devices. After the board is lowered to contact the spring-loaded magazines, the magazines push the chips onto the epoxy spots. This procedure is many times faster than standard axial/radial-leaded insertion. Also, the mounting method eliminates the need for lead inspection and straightening, as well as shutdowns that result from the misalignment of leads.

With the air-tweezer system, tape reels of chip capacitors, transistors and resistors are mounted side-by-side in an automatic air-tweezer machine, which has been programmed to place various devices on the PC board. One arm places a small drop of epoxy on the board. Immediately thereafter, another arm mounts the component in place.

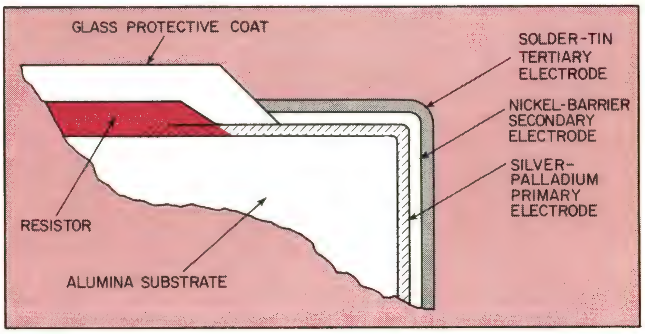
Insertion speed with the air-tweezer method is 0.4 second per chip placement—about twice as fast as standard insertion but considerably slower than magazine insertion. However, the air-tweezer method is a better choice than magazine insertion, for runs of up to a few hundred boards, because design changes involve less downtime.

Once cured, the PC boards can be broken apart, cassette-loaded and prepared for the automatic insertion of other components. Standard equipment will mount other components without harming the chip components. The boards may then be fluxed (foam flux works better than brush or roller fluxing) and flow-soldered.

Preheating is not required for the MCR-18. However, if preheating is necessary for other components, preheating temperatures should not exceed 100 to 150 C for two to three minutes. Cleaning may be done with Freon TMC or trichloride solvents (resin flux), or it can be done with ultrasonic methods using de-ionized water (acid flux).■■



1. The new MCR-18 chip resistor (a) can be mounted with its resistive element up or down. With a conventional chip resistor (b), the electrodes do not extend around the ends of the device.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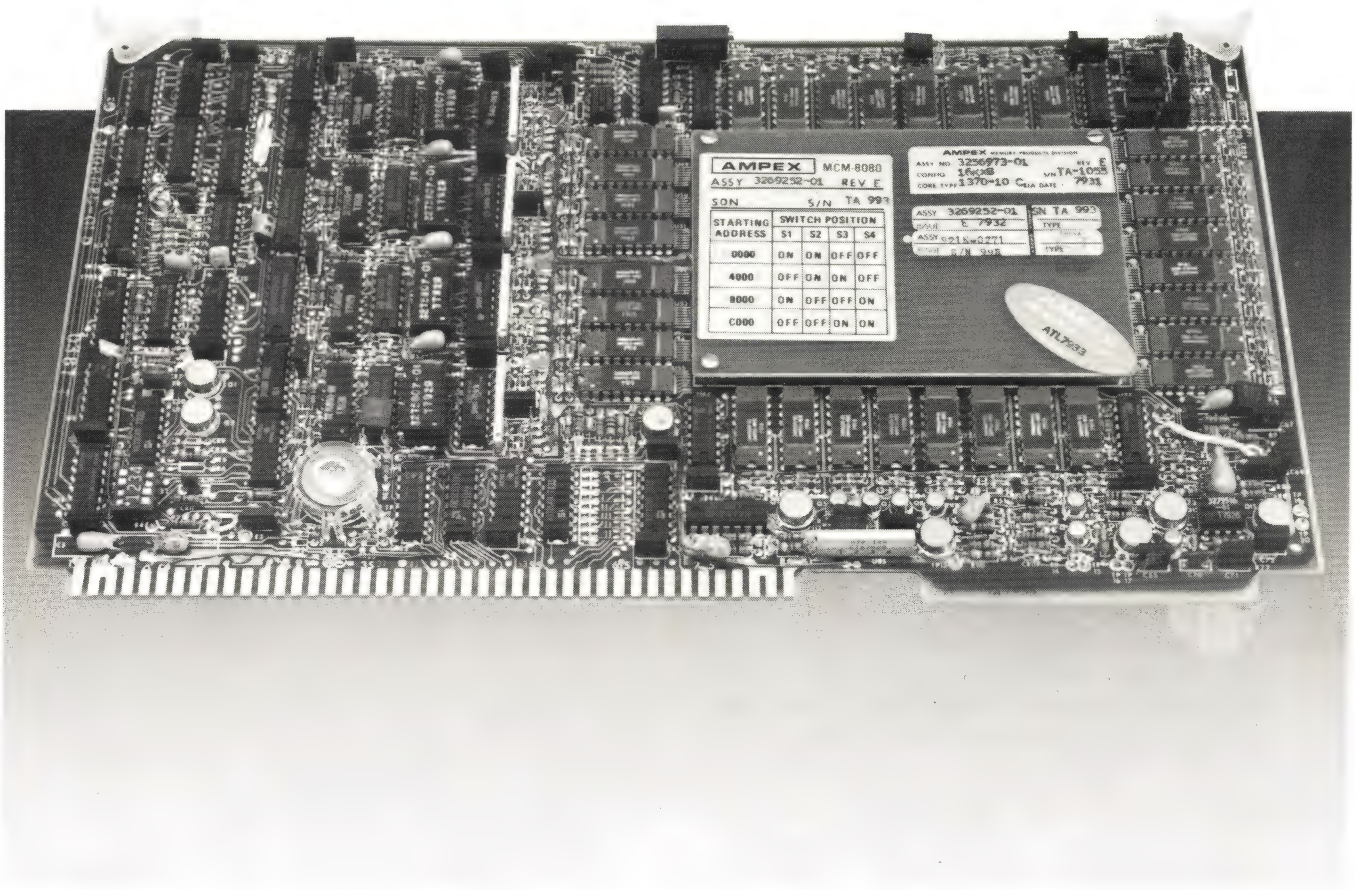

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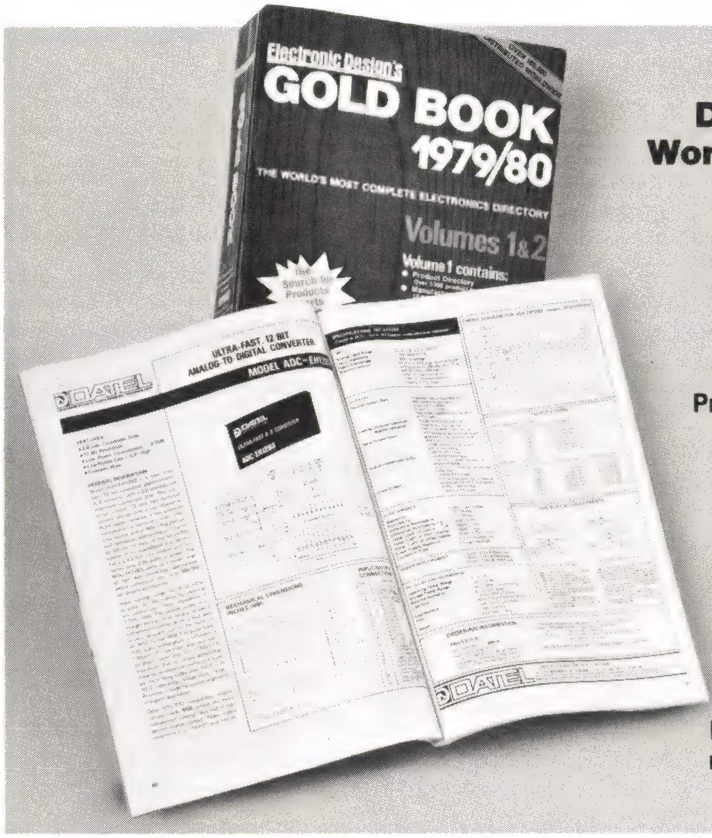
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CIRCLE NUMBER 48

Computer modeling of pulse-width modulators simplifies analysis of switching regulators

As pulse-width modulators (PWMs) figure ever more prominently in power supplies, the need grows for computer models of the switching and control elements that permit a quick, accurate, low-cost evaluation of the switching-regulator design.

Now, with computer circuit-analysis packages that use Fortran statements and subroutines—Computer Sciences Corp.'s TRAC and CDC SYSCAP II are two examples—a PWM-inverter model can be developed and used simply as a subcircuit. Analysis—dc, small-signal ac, large-signal transient, open and closed-loop—can be performed interactively at a computer time-sharing terminal.

The main problem in switching regulator analysis is modeling the PWM inverter. An inverter acts as a multiplier whose average output voltage equals the dc input voltage multiplied by the duty cycle—both of which change dynamically. Most currently available circuit analysis packages cannot model a multiplier.

The improved model is based on Middlebrook's averaged universal computer model,[1] which uses state-space averaging techniques to show that a switching converter can be modeled as an ideal dc/dc transformer whose turns ratio is controlled by the duty cycle. However, using Middlebrook's small-signal ac model (ELECTRONIC DESIGN, Nov. 22, 1978, p. 132) switchers can be analyzed on generally available circuit programs such as ECAP or SPICE for open and closed loops.

On the other hand, CSC TRAC, with its Fortran statement and subroutine capability, can be used to simulate Middlebrook's large-signal model. To properly simulate switching-regulator operating conditions in TRAC, start by modeling the PWM inverter.

Constructing the PWM model

Basically, the PWM inverter model in Fig. 1 is an ideal dc/dc transformer whose turns ratio equals the duty cycle of the controller times the transformer's actual turns ratio. This combines the inverter switching transistor and transformer in a single, easy-to-use subcircuit model.

One input to the transformer model, the duty cycle D, is calculated dynamically as an output of an SG1524 pulse-width modulator IC. Current sources J1, J2, JA and JB are partial derivative sources that must be used for dynamically multiplying variables. These sources give Newton-Raphson iterations and good covergence for dc and large-signal transient analysis. They also provide small-signal ac gains at a particular dc operating point.

A computer listing (CSC TRAC) for a PWM inverter is given in Fig. 2. Partial derivative sources and outputs of the model are calculated dynamically by the Fortran statements in lines 170 through 220.

For the PWM transformer model of Fig. 1, the inverter output voltage, V_2, is given by

$$V_2 = DV_1 (N_2/N_1) - R_o I_2, \tag{1}$$

and the input current, I_1, is given by

$$I_1 = DI_2 (N_2/N_1) \tag{2}$$

where V_1 is the input voltage,
I_2 is the output current,
R_o is the output resistance,
N_1 is the number of primary turns,
N_2 is the number of secondary turns,
D is the instantaneous duty cycle.

To use the model, simply specify the input and output nodes, 1 to 4, the controlling node, 5, and the transformer turns and output resistance. As shown in Fig. 1, the model sets default values for parameters P1 to P3. These parameters can be reset when the subcircuit model is called from the main circuit: P1 = N_1, the transformer primary turns; P2 = N_2, the transformer secondary turns; P3 = R_o, the output resistance.

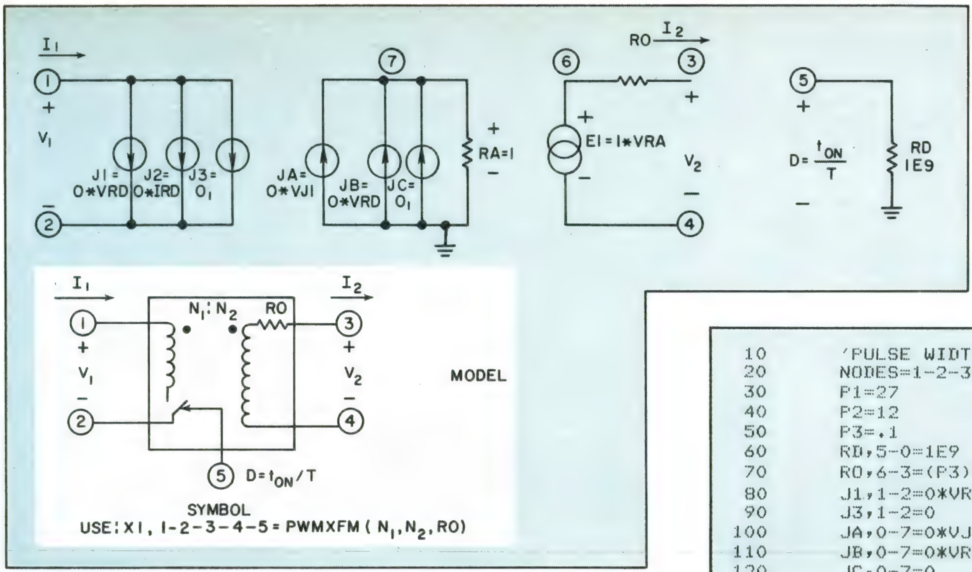
The voltage, VRD, across resistor RD (Fig. 1) is the duty cycle, D. Similarly, voltage VJ1 across current source J1 is the input voltage V_1. And current IRO through resistor R_o is the output current I_2. Now the voltage VRA across resistor R_A is the product of input voltage, duty cycle and turns ratio:

$$\begin{aligned}\mathbf{VRA} &= \mathbf{RA * (JA * VJ1 + JB * VRD + JC)}\\ &= \mathbf{VRD * VJ1 * P2/P1}\\ &= DV_1 (N_2/N_1) \end{aligned} \tag{3}$$

Therefore, the output voltage from Eq. 1 can be written as

$$V_2 = \mathbf{VRA - IRO\ P3}$$

Vincent G. Bello, PhD, Senior Research Engineer, Norden Systems, Norwalk, CT 06856.



1. An ideal dc/dc transformer is the pulse-width modulator (PWM) inverter model for the TRAC program, which can be used as a subcircuit of a switching regulator.

$$= DV_1\ (N_2/N_1)\ -\ I_2R_2 \qquad (4)$$

and the input current, the sum of the currents in sources J1, J2 and J3, from Eq. 2, is

$$\begin{aligned} I_1 &= J1 * VRD + J2\ IRO + J3 \\ &= \mathbf{VRD * IRO * P2/P1} \\ &= DI_2\ (N_2/N_1) \qquad (5) \end{aligned}$$

With similar procedures, the current sources can be modeled for a TRAC program.

Modeling nonlinear sources

In TRAC, the name of a controlled source is set equal to the value of its transconductance. For example, current IJ1 through voltage-controlled current source J1 is equal to J1 * VRD.

Controlled source J1 (lines 80 and 170 in Fig. 2) models variations of the input current with duty cycle. From Eq. 2,

$$\begin{aligned} J1 &= \partial I_1/\partial D \\ &= I_2\ (N_2/N_1) \\ &= \mathbf{IRO * P2/P1} \qquad (6) \end{aligned}$$

Controlled source J2 (lines 140 and 180) models variations of input current with the output current:

$$\begin{aligned} J2 &= \partial I_1/\partial I_2 \\ &= D\ (N_2/N_1) \\ &= \mathbf{VRD * P2/P1} \qquad (7) \end{aligned}$$

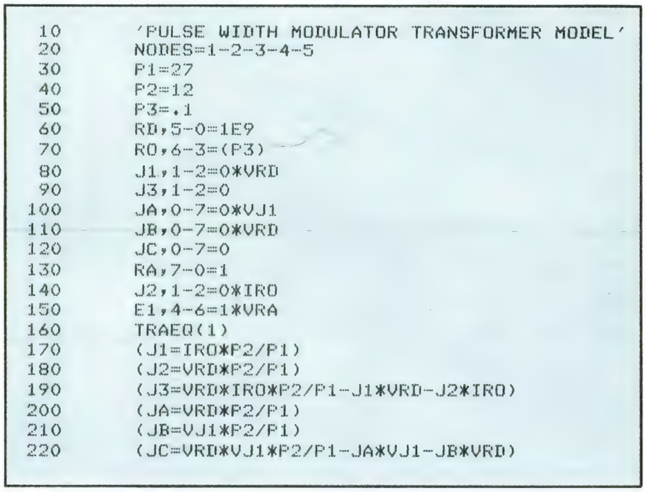
Controlled source J3 (lines 90 and 190) calculates the operating point based on the desired input current I_1 and the variations:

$$\begin{aligned} I_1 &= IJ1 + IJ2 + IJ3 \\ &= \mathbf{VRD * IRO * P2/P1} \qquad (8) \end{aligned}$$

Now write equations for controlled sources JA, JB and JC. Since JA models variations of output voltage to input voltage, its equation is

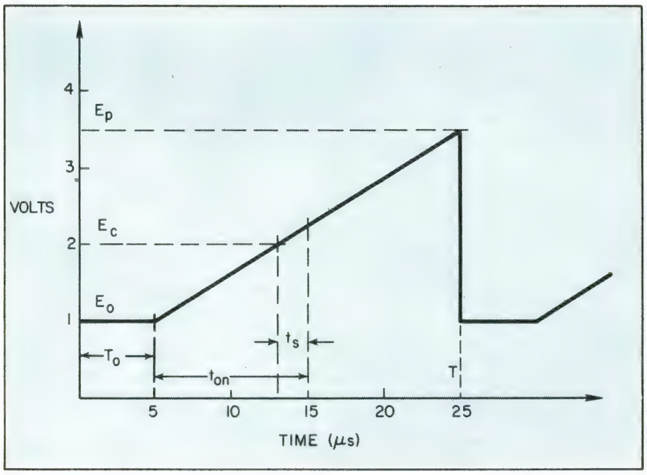
$$\begin{aligned} JA &= \partial V_2/\partial V_1 \\ &= D\ (N_2/N_1) \\ &= \mathbf{VRD * P2/P1.} \qquad (9) \end{aligned}$$

Source JB models variations of output voltage with duty cycle, or



```
 10        'PULSE WIDTH MODULATOR TRANSFORMER MODEL'
 20        NODES=1-2-3-4-5
 30        P1=27
 40        P2=12
 50        P3=.1
 60        RD,5-0=1E9
 70        RO,6-3=(P3)
 80        J1,1-2=0*VRD
 90        J3,1-2=0
100        JA,0-7=0*VJ1
110        JB,0-7=0*VRD
120        JC,0-7=0
130        RA,7-0=1
140        J2,1-2=0*IRO
150        E1,4-6=1*VRA
160        TRAEQ(1)
170        (J1=IRO*P2/P1)
180        (J2=VRD*P2/P1)
190        (J3=VRD*IRO*P2/P1-J1*VRD-J2*IRO)
200        (JA=VRD*P2/P1)
210        (JB=VJ1*P2/P1)
220        (JC=VRD*VJ1*P2/P1-JA*VJ1-JB*VRD)
```

2. The TRAC listing for the PWM transformer in Fig. 1 calculates partial-derivative sources dynamically with Fortran statements 170 through 220.



3. Duty-cycle relationships for an SG1524 PWM IC are illustrated by this sawtooth waveform, which is the input voltage to the IC's comparator.

$$\begin{aligned} JB &= \partial V_2/\partial D \\ &= V_1\,(N_2/N_1) \\ &= \mathbf{VJ1 * P2/P1} \end{aligned} \qquad (10)$$

Now JC calculates the operating point, and the output voltage is

$$\begin{aligned} \mathbf{VRA} &= \mathbf{IJA + IJB + IJC.} \\ &= \mathbf{VRD * VJ1 * P1/P2,} \end{aligned}$$

which gives the output voltage VRA $- I_2 R_o$.

The Fortran statements on line 160 are evaluated at each iteration for dc and transient solutions, and converge rapidly to a solution. Without the partial derivative sources, this would not happen. For ac small-signal analysis, the dc operating point is calculated, and the controlled sources provide the ac gains evaluated at the dc operating point.

Control amplifier modeling

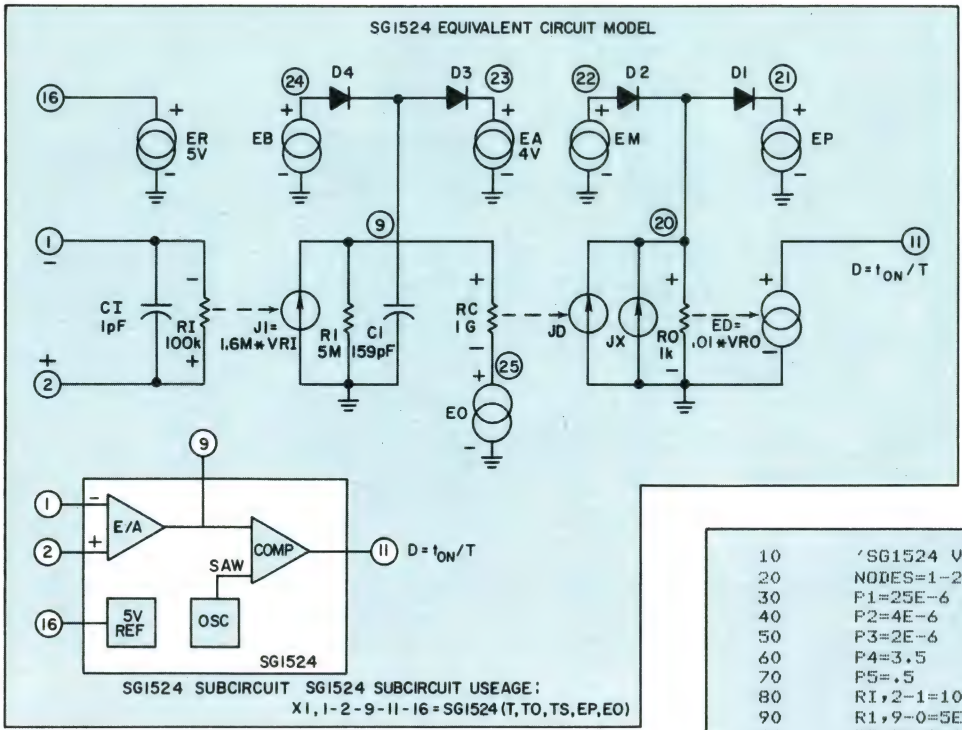
While the details of nonlinear device modeling should be understood in their own right, the model itself can be handled more simply—one statement is required to specify the node connections and parameters. Then a buck power stage, with or without a real transformer, can be simulated.

To close the control loop in a switching regulator, define the relationship of the error amplifier's control voltage to the duty cycle. For an SG1524 PWM, the duty cycle is expressed as

$$\begin{aligned} D &= t_{on}/T \\ &= \frac{t_s}{T} + \frac{E_c - E_o}{E_p - E_o}\left[\frac{T - T_o}{T}\right] \end{aligned} \qquad (11)$$

where t_{on} is the transistor on time,
T is the switching period,
T_o is the dead time,
t_s is transistor storage time,
E_c is the control voltage,
E_p is the peak sawtooth voltage,
E_o is the minimum sawtooth voltage.

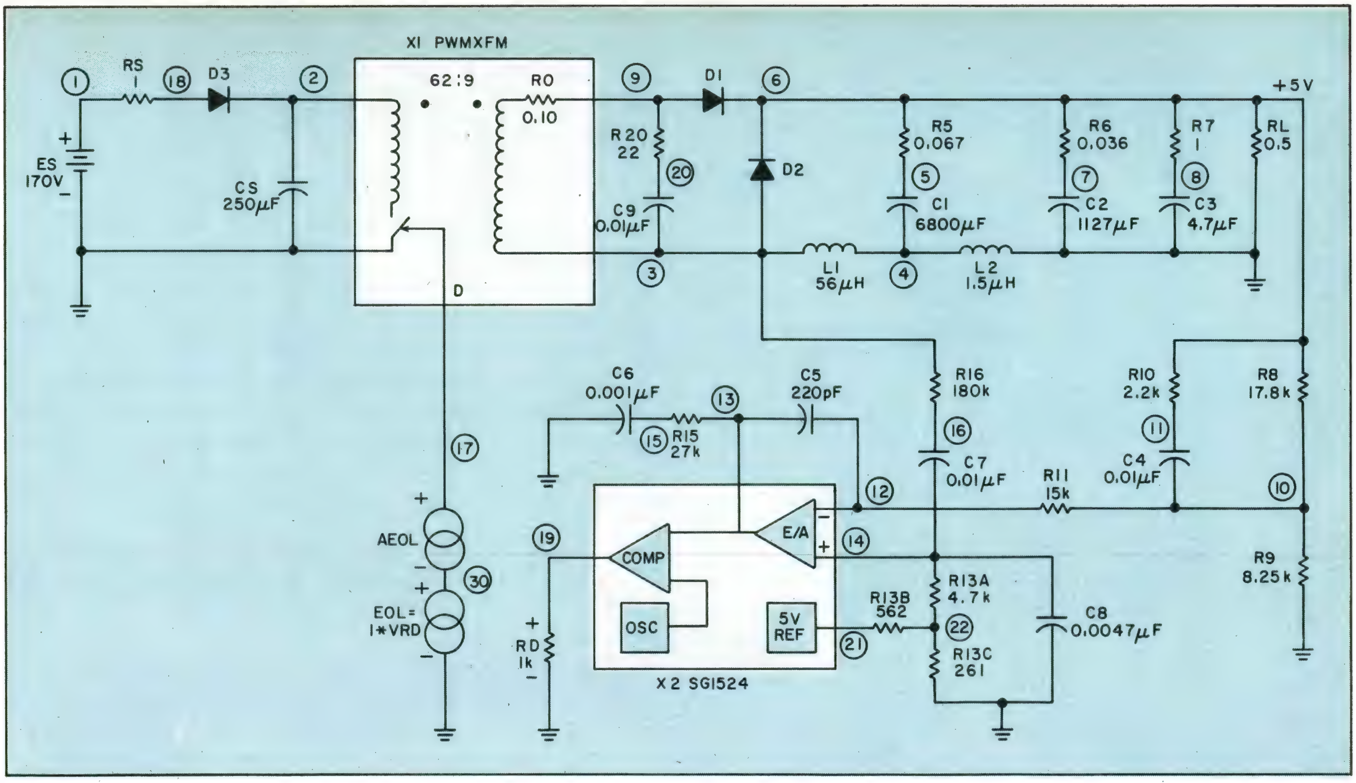
Fig. 3 shows the relationship of these parameters in the typical sawtooth waveform that appears at the input of the 1524's comparator.



4. One subcircuit model used by the TRAC program is for an SG1524 PWM IC. The SG1524 model and PWM inverter model connect at pin 11, the duty-cycle output.

```
 10     'SG1524 VOLTAGE REGULATOR MODEL'
 20     NODES=1-2-9-11-16
 30     P1=25E-6
 40     P2=4E-6
 50     P3=2E-6
 60     P4=3.5
 70     P5=.5
 80     RI,2-1=100E3
 90     R1,9-0=5E6
100     RO,20-0=1000
110     RC,9-25=1E9
120     EO,0-25=(P5)
130     EA,0-23=4
140     EB,0-24=(P5-.1)
150     CI,2-1=1E-12
160     C1,9-0=159.2E-12
170     J1,0-9=(1.6E-3*300/TEMP)*VRI
180     ED,0-11=.01*VRO
190     ER,0-16=5
200     JD,0-20=(.1*(P1-P2)/((P4-P5)*P1))*VRC
210     JX,0-20=(.1*P3/P1)
220     EP,0-21=(100*(P1+P3-P2)/P1)
230     EM,0-22=(100*P3/P1)
240     D1,20-21=1N3605
250     D2,22-20=1N3605
260     D3,9-23=1N3605
270     D4,24-9=1N3605
```

5. The complete TRAC listing for the SG1524 in Fig. 4 allows easy entry of the time and voltage parameters in Eq. 11. Parameters, P1 through P5, are called default values.



6. Both the PWM inverter and SG1524 subcircuit models are entered into this complete switching regulator circuit. **Equivalent to a circuit already presented in ELECTRONIC DESIGN (see text), the newer circuit is modeled for TRAC.**

Fig. 4 illustrates the 1524's subcircuit model, including both the error amplifier and pulse-width modulator. At the model's output (pin 11), the duty-cycle signal is connected to the duty-cycle input of the PWM inverter model. To use the model, simply give the external node connections and parameter values as shown in Fig. 4.

The impedance looking into the 1524's input is modeled by RI and CI in Fig. 4. Open-loop gain A_{OL} is given by the voltage-controlled current source J1 and resistance R1:

$$A_{OL} = \mathbf{J1} * \mathbf{R1} = 8000$$

Capacitor C1 gives the error amplifier bandwidth,

$$BW = (2\pi R1C1)^{-1} = 200 \text{ Hz}.$$

Eq. 11 is modeled by sources JD, JX and EO, giving the percent duty cycle at node 20. Source ED then gives the fractional duty cycle at node 11. Sources EP and EM limit the maximum and minimum percent duty cycle from Eq. 11, while EA and EB limit the voltage at pin 9 of the error amplifier. ER is a 5-V reference model, from pin 16 of the 1524.

The complete TRAC program listing for modeling an SG1524 is given in Fig. 5. The parameters, from Eq. 11, are defined as follows: P1 = T, P2 = T_o, P3 = t_s, P4 = E_p, P5 = E_o. Note in line 170 that source J1 is a temperature-dependent model—it models the temperature variation of the error amplifier's open loop gain:

$$A_{OL} = \frac{q \cdot I_c R_L}{2kT}$$

```
 10       '5V , 10A SWITCHING REGULATOR EXAMPLE'
 20       RS,1-18=1
 30       R5,6-5=.067
 40       R6,6-7=.036
 50       R7,6-8=1
 60       R8,6-10=17.764E3
 70       R9,10-0=8.25E3
 80       R10,6-11=2.2E3
 90       R11,10-12=15E3
100       R13A,14-22=4.7E3
110       R13B,21-22=562
120       R13C,22-0=261
130       R15,13-15=27E3
140       R16,3-16=180E3
150       R20,9-20=22
160       RD,19-0=1E3
170       RL,6-0=.5
180       C1,5-4=6800E-6
190       C2,7-0=1127.5E-6
200       C3,8-0=4.7E-6
210       C4,11-10=.01E-6
220       C5,13-12=220E-12
230       C6,15-0=.001E-6
240       C7,16-14=.01E-6
250       C8,14-0=.0047E-6
260       C9,20-3=.01E-6
270       CS,2-0=250E-6
280       L1,3-4=56.3E-6,.01
290       L2,4-0=1.52E-6
300       EOL,0-30=1*VRD
310       AEOL,30-17=0
320       X1,2-0-9-3-17=PWMXFM(62.,9.,.1)
330       X2,12-14-13-19-21=SX1524
          (31E-6,16.2E-6,.5E-6,3.5,.7)
340       D1,9-6=1N3605
350       D2,3-6=1N3605
360       D3,18-2=1N3605
370       DEFAULTS,IDC=50,TOMIN=.1E-9
380       NOCTL
```

7. All the components of the switching-regulator-equivalent circuit in Fig. 6 are listed in this TRAC file. Line 320 is the PWM transformer, while line 330 contains the data for the 1524.

```
 10       !LIMIT USE:50 LINES:2000
 20       !DO TRAC.N
 30       *
 40       *
 50       *
 60       INCLUDE,SWTREG
 70       ES,0-1=170
 80       AEOL=1
 90       FREQ=10(1)10E3
100       PRINT,PLOT(DB),VRD,VRL,VN13
110       TRAEQ(1)
120       (PRINT *,VN6,VN12,VN13,VN14,VN19)
130       (EOL=1.)
140       (IF(ACFLG)EOL=0.)
210       !LIMIT USE:50 LINES:2000
220       !DO TRAC.N
230       *
240       *
250       *
260       INCLUDE,SWTREG
270       ES,0-1=170
280       SENSITIVITY(.1),VN6
290       PRINT,VRL,VRD,VN13,VRIX2,IL1
310       !LIMIT USE:50 LINES:2000
320       !DO TRAC.N
330       *
340       *
350       *
360       INCLUDE,SWTREG
370       ES,0-1=170
380       RL=1
390       TJL,6-0=0,0,1E-6,5,1,5
400       INTERVALS=1E-9,20E-6,500E-6
410       PRINT(1),PLOT,VRL,VRD,VN13,VRIX2,IL1
510       !LIMIT USE:50 LINES:2000
520       !DO TRAC.N
530       *
540       *
550       *
560       INCLUDE,SWTREG
570       TES,0-1=0,170,1E-6,190,1,190
580       INTERVALS=1E-9,50E-6,1000E-6
590       PRINT(1),PLOT,VN2,VRL,VRD,VN13,VRIX2,IL1
592       P1=(VRL-5.)
594       P2=(VRD-.295)
596       PRINT,PLOT,P1,P2
610       !LIMIT USE:50 LINES:2000
620       !DO TRAC.N
630       *
640       *
650       *
660       INCLUDE,SWTREG
670       ES,0-1=170
680       SENSITIVITY(.1),VN6
690       PRINT(DB),VRD,VRL,VN13
700       FREQ=4E3
710       AEOL=1
720       TRAEQ(1)
730       (EOL=1.)
740       (IF(ACFLG)EOL=0.)
```

8. Complete analysis of a switching regulator—ac open loop, dc sensitivity, load and line transients, and ac sensitivity—is handled by this TRAC control file. Because of Fortran programming and subroutines, CSC TRAC is one of the most complete circuit analysis programs available.

Now all the modeling is complete, and a switching regulator design can be simulated.

Putting it all together

To do that, combine the PWM inverter and control amplifier subcircuit models with the output filter circuit and error amplifier compensation. Then analyze the model for open and closed-loop dc and ac, and transient responses. No circuit measurements are necessary to evaluate a design.

All model parameters can be found in data sheets, or can be estimated before actual hardware is available. When hardware is available, secondary effects and parasitics can be measured to characterize the circuit further and enhance the model.

For comparison, a good switching regulator to analyze is the circuit used by Richard Keller in the Nov. 22, 1978 issue of ELECTRONIC DESIGN. The schematic is on p. 134 of that article. An equivalent circuit of that regulator is given in Fig. 6 of this article.

Both the PWM inverter and SG1524 are replaced by their subcircuit models, while the remaining components are taken directly from the schematic. TRAC coding for the circuit is given in Fig. 7. Line 320 of the listing, the PWM inverter model, uses the transformer turns and an equivalent output resistance for the transformer, to give the following parameters: $N_1 = 62$, $N_2 = 9$, and $R_o = 0.1\ \Omega$.

It's necessary to estimate the output resistance from the expected open-loop-gain voltage drop of the transformer, while it is under load. If hardware is available, measurements should be made to refine this parameter.

The source voltage E_s is defined as

$$\begin{aligned} E_s &= \sqrt{2}\ E_{rms} \\ &= 170\ \text{V}. \end{aligned}$$

Line 330 of the program is the 1524 model, and data-sheet specifications are used to determine parameters T, T_0, E_p and E_o. In addition, the switching transistor's storage time is estimated from a data sheet.

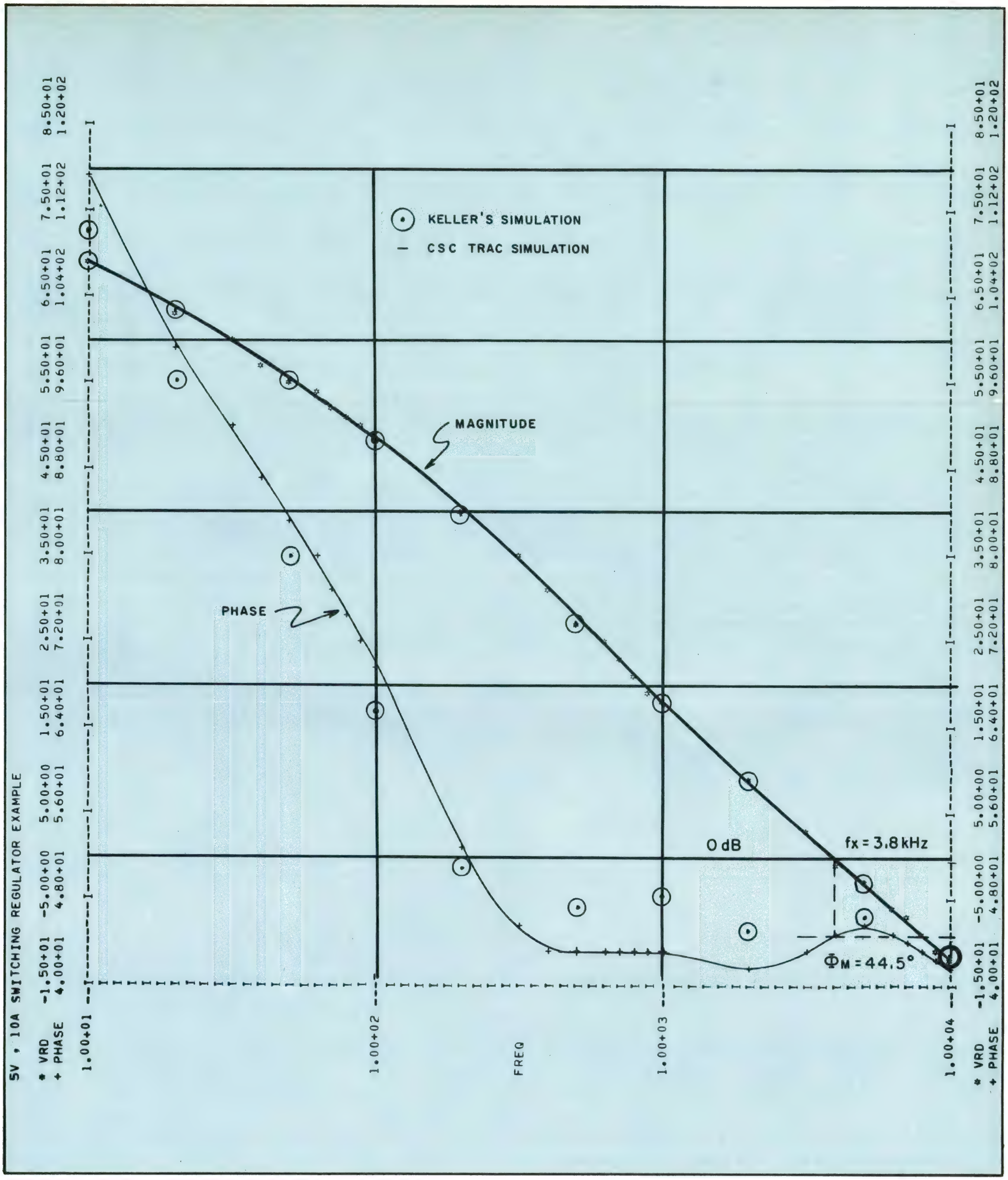
Switching period and dead time are set by selecting a timing resistor, R_T, of 3.3 kΩ and a timing capacitor, C_T, of 0.047 μF, so that using one drive of the 1524,

$$\begin{aligned} T &= 2\ R_T\ C_T \\ &= 31\ \mu\text{s}, \\ T_0 &= R_T\ C_T + 0.7\ \mu\text{s} \\ &= 16.2\ \mu\text{s}. \end{aligned}$$

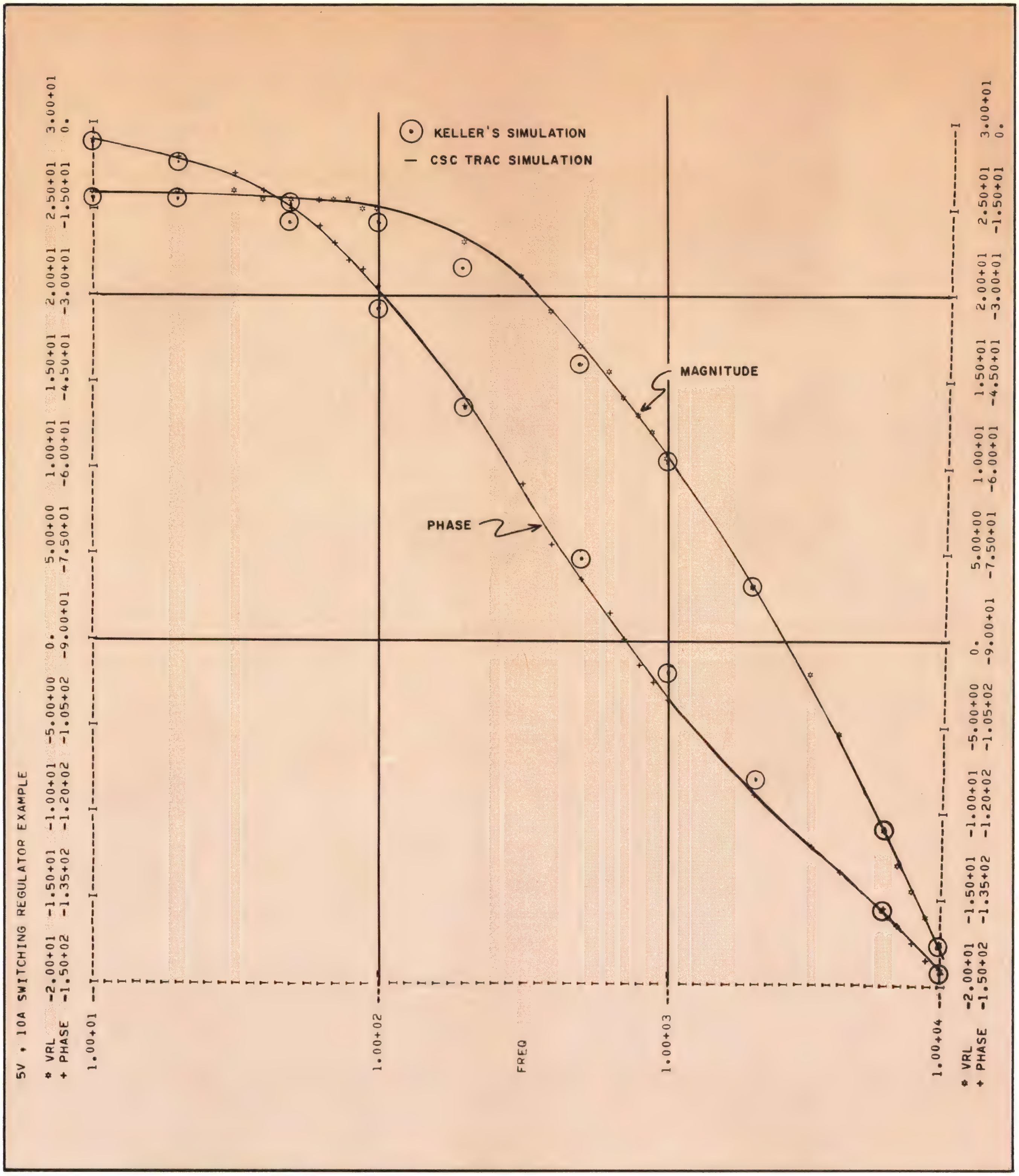
Typical sawtooth levels are $E_p = 3.5$ V and $E_o = 0.7$ V.

For this design, the storage time is estimated at 0.5 μs. The equivalent series resistance of the output capacitors is important because ESR generally introduces a zero at low frequencies (1 to 10 kHz), and this improves the phase margin. Resistors R5, R6 and R7 model the capacitors' ESRs. Note also that ESR can vary widely from nominal, and at low temperatures increases by a factor of four. Choosing too low an ESR can cause stability problems.

At this point, the control file illustrated in Fig. 8



9. This ac open-loop plot of the switching-regulator-equivalent circuit is generated by the control file in Fig. 8. The Keller results show how closely the large and small-signal models correlate.



10. A plot produced by the TRAC program for frequency response provides additional evidence of the good correlation between this technique and Keller's.

can be used to produce a series of analyses. It can be used interactively for fast turnaround or, to reduce costs, run in a batch mode.

The results come in

The program, called a control file, runs the following analyses: ac open loop, dc sensitivity, load transient, line transient and ac sensitivity. What's more, ac or dc worst-case, failure and Monte Carlo analyses can also be done.

The first run, shown in the plot of Fig. 9, is an ac open-loop analysis from 10 Hz to 10 kHz, and comes from lines 10 through 140 in the control file. For comparison, Keller's results are shown in the same plot. In Fig. 6, ac source AEOL and controlled source EOL are included to open the loop for ac analysis and keep it closed for dc analysis to determine the dc operating point.

With the following Fortran statements, it is easy to run ac open-loop analyses at a desired dc closed-loop operating point:

- Line 80 sets AEOL equal to 1 for ac open loop.
- Line 130 sets the gain of EOL to 1 for dc analysis.
- Line 140 sets EOL to 0.0 for ac analysis, opening the loop.
- Line 120 prints out the dc iterations and, as a check, the final dc operating point.

For a load current of 10 A, the duty cycle, D, is calculated to be D = VN19 = 29.5%. At node 13, the control voltage VN13 equals 2.33 V. Both the crossover frequency of 3.8 kHz and phase margin of 44.5° in Fig. 9 agree closely with Keller's results. And contrary to previous findings, it is not correct to include a pole at half the switching frequency to account for delay in the modulator.

Gain and phase measurements made on the 1524 modulator section with an HP3582A spectrum analyzer show no phase shift up to the switching frequency.

Fig. 10 shows the frequency response from the output of the SG1524 to the 5-V output, along with Keller's results. The low frequency gain, $\partial V_{out}/\partial D$, gives the response of the PWM inverter model and output filter when driven from the duty-cycle input.

These two plots only begin to demonstrate the program's versatility. With the remaining steps of the control file, dc sensitivity, transient responses and ac open loop sensitivity analyses can be generated. ■■

References

1. Middlebrook, R. D., and Cuk, S., "A General Unified Approach to Modeling Switching-converter Power Stages," IEEE Power Electronics Specialists Conference, 1976 Record, pp. 18-34.

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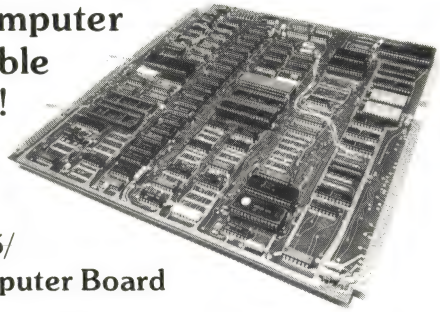

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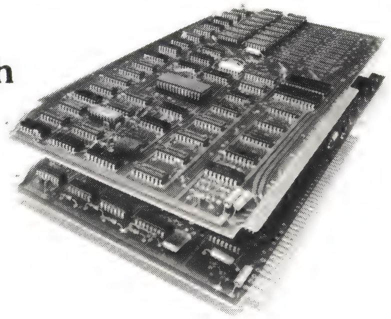

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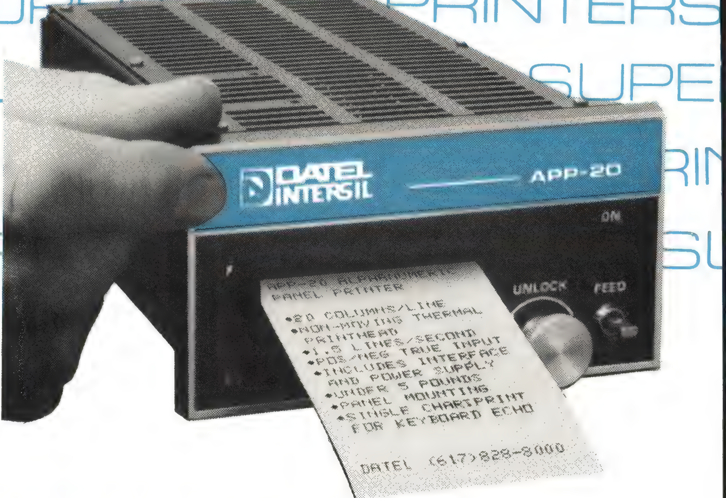
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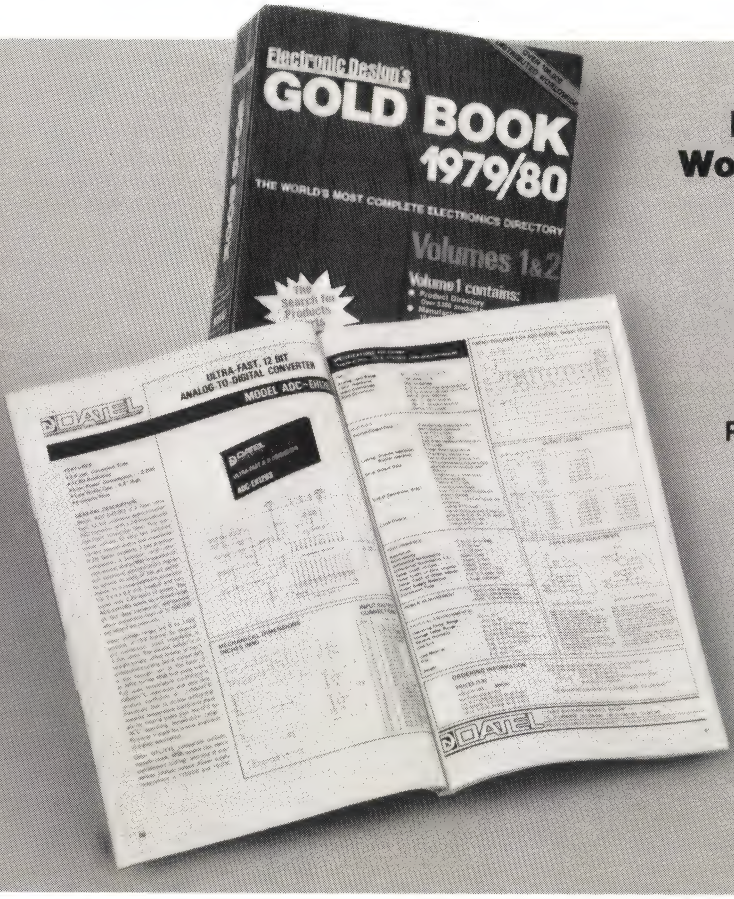
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AIP-40 Type 2 (Serial)	"	"	"	"	"	2-wire 20 mA loop or RS-232-C	"	120-char. buffer	From **$690**
DPP-Q7	Panel-mnt. dec/hex thermal with all electronics	7 (6 plus sign)	240 lines/ min.	Numerals or Hexadecimal	Non-impact inkless thermal 7-segment, 1.75" paper	Full Parallel latched BCD, pos/neg true	115/230 VAC built-in	4.4 lb, 105 cu. in. miniature	From **$509**
APP-20 (Parallel)	Panel-mnt. alpha-thermal with all electronics	20	72 lines/ min.	96 alpha-numeric (Full upper and lower case)	Non-impact inkless thermal 5 x 7 dot matrix, 2.3" paper	8-Bit Parallel Asynchronous, 20-char. register, pos/neg true	115/230 VAC switchable, built-in. Optional 12 VDC @ 1A	4.25 lb, 105 cu. in. miniature, selectable inverted (text) printing	**$730**
APP-20 (Serial)	"	"	"	"	"	2-wire 20mA loop, 300VRMS, 100MΩ or RS-232-C Serial, 75 to 9600 baud, 9, 10, 11 bits, 20-char. reg.	"	"	**$880**

CIRCLE NUMBER 50

Intelligent processors transmit asynchronous data without errors

For efficient line-use and transparency to the user, relegate error protection to a turnkey network processor that also concentrates asynchronous data streams statistically. Data from several sources can be concentrated and then placed into error-protection envelopes for fast delivery, using designs based on the International Consultative Committee for Telegraphy and Telephony (CCITT) X.25 Recommendation.

In data communications, errors incurred in transmission are the scourge of the communicator. Developments in transmission systems, techniques and equipment have not yet perfected communication facilities to eliminate completely the corruption of data through transmission errors.

Synchronous transmissions depend upon terminal-host protocols; and, at higher data rates—2400 bps and above—error detection and recovery become more critical. The retransmission of large volumes of data wastes costly time, materials and resources.

The most popular methods for error correction use some form of the half-duplex Stop-And-Wait Acknowledge Request (ARQ) protocol, such as IBM's Bisync. More effective are full-duplex Go-Back-N ARQ protocols (e.g., SDLC), which are gaining acceptance.

To counteract excessive transmission delays in sophisticated systems (for example, in satellite circuits), Selective-Repeat ARQ schemes are used. Such schemes are typically used in medium to high-speed batch or RJE applications.

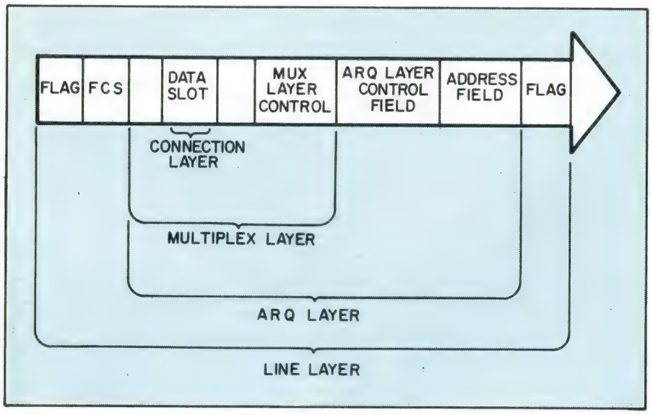
In asynchronous communication, many terminals operate without the benefit of error protection. However, for those applications which mandate error protection, several techniques are available. One method, blocked format, creates messages or information blocks and appends some sort of check character to the transmission, as in magnetic data recording. Usually the checking mechanism uses a single, longitudinal, redundancy-check (parity) character.

Though not as powerful as the 16-bit cyclic redundancy check (CRC) used in synchronous protocols, longitudinal parity—used with an end-to-end protocol—can test for and help the system recover from transmission errors. Because end-to-end, asynchronous, error protection requires an intelligent terminal or terminal-control unit and because the host must have the appropriate software to support the protocol, the necessary hardware and software represents a cost trade-off that can be excessive in some environments.

Echoplex or echo-back is another scheme that is often used: A character received at a processing facility is sent back (echoed) to the originating terminal, visually verifying that the character sent was correctly received. The user reenters or edits erronous characters. Unfortunately, this method of error protection has three basic shortcomings:

- Users must verify data entry.
- Corrupted echoed characters are unprotected.
- Protection is undirectional only—data from a computer to a user is not verified, unless the receiving user knows what the output should be or suspects the received results.

In today's distributed-processing environments—



1. **The internodal multiplex port protocol, used in Codex's 6010 Intelligent Network Processor, consists of line, ARQ, multiplex and connection layers. The protocol is a subset of the packet-switching Recommendation X.25 Level 2.**

Dave Moore, Group Product Manager, Codex Corp., 20 Cabot Blvd., Mansfield, MA 02048.

where terminals are commonly clustered together—error protection is only one part of the data-communications puzzle. User transparency and efficient line use are also important. The previously discussed error protection schemes are concerned with single-channel transmission. In multichannel systems, multiplexing can also be combined with error-protection to boost transmission efficiency. Both statistical multiplexing and data concentration use link-access procedures to provide an error-protected envelop for transmitting data.

Enhanced TDM dedicates time slots

Conventional, character-interleaved, time-division multiplexing (TDM) dedicates time slots statically and assigns the attached terminals to fixed time slots on a high-speed link. The basis for assigning time slots is the number of terminals, their speed and the aggregate link speed. Changes in allocation require reconfiguration. Traditional (nonintelligent) TDM constrains the sum of the terminal data rates to a speed less than, or at best equal to, the link rate, and without the benefit of run protections.

Statistical concentration—an enhanced type of TDM—allocates the link bandwidth statistically and dynamically in response to terminal activity as information is presented. Inactive terminals get no space. Only terminals with data to be transmitted are serviced. Statistical (intelligent) TDMs handle aggregate terminal data rates that exceed the link rate, often by two to four times, because the inactive terminals are not taking line space. Since some terminals operate only 5 to 10% of the time, a dramatic advantage to statistical multiplexing can result.

For example, Codex's 6010 Intelligent network processor (INP) places data from up to 30 asynchronous input lines onto a single, high-speed, synchronous output line. The INP's highly structured Multiplex Port Protocol (MPP) aids transmission efficiency and provides error protection over a full-duplex link. Both data and control signals are passed to maintain user transparency. The MPP addresses ports explicitly and defines its fields rigidly, so that software-driven processors (other than Series-6000) can interpret and demultiplex its frames.

The INP's internodal protocol derives much of its power from its packet-transmission scheme, which is based (in part) on the X.25 Recommendation of the CCITT. The X.25 Recommendation is officially titled "Interface between Data-Terminal Equipment for Terminals Operating in the Packet Mode." It encompasses three levels: Level 1 for physical interface characteristics; Level 2 for link-access procedure; and Level 3 for the packet-level interface.

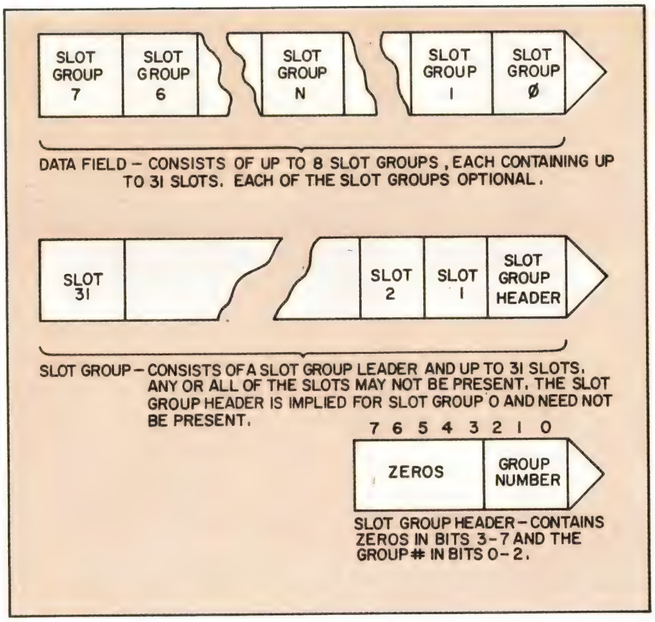
Data travels in error-protected envelops

The access procedures of Level 2, in particular, provide an error-protected envelope for transmitting data between network nodes. The information interchange between nodes is via multiplexed user data frames, bounded by a compatible subset of X.25 Level 2. This internodal Multiplex Port Protocol consists of four layers, as Fig. 1 shows schematically.

- Layer 1 is the Line layer for transmission requirements, transparency, interframe-idle fill and frame pacing.
- Layer 2 is the ARQ layer for error recovery, frame identification and sequence control.
- Layer 3 is the Multiplex layer containing control and data fields.
- Layer 4 is the Connection layer for user data that are transmitted between nodes.

MPP frames are bounded by opening and closing flags. A flag has the unique pattern: 01111110. The Line layer maintains transparency by appropriately inserting and deleting ZEROs to assure that data or control characters are not misinterpreted as flags. Thus, the transmitter inserts a ZERO following any sequence of five ONEs; the receiver, on the other hand, deletes the ZERO.

In addition to this ZERO stuffing and stripping, the Line layer verifies the frame-check sequence, detects


SLOT GROUP 7
SLOT GROUP 6
SLOT GROUP N
SLOT GROUP 1
SLOT GROUP 0
DATA FIELD – CONSISTS OF UP TO 8 SLOT GROUPS, EACH CONTAINING UP TO 31 SLOTS. EACH OF THE SLOT GROUPS OPTIONAL.
SLOT 31
SLOT 2
SLOT 1
SLOT GROUP HEADER
SLOT GROUP – CONSISTS OF A SLOT GROUP LEADER AND UP TO 31 SLOTS. ANY OR ALL OF THE SLOTS MAY NOT BE PRESENT. THE SLOT GROUP HEADER IS IMPLIED FOR SLOT GROUP 0 AND NEED NOT BE PRESENT.
7 6 5 4 3 2 1 0
ZEROS
GROUP NUMBER
SLOT GROUP HEADER – CONTAINS ZEROS IN BITS 3-7 AND THE GROUP # IN BITS 0-2.

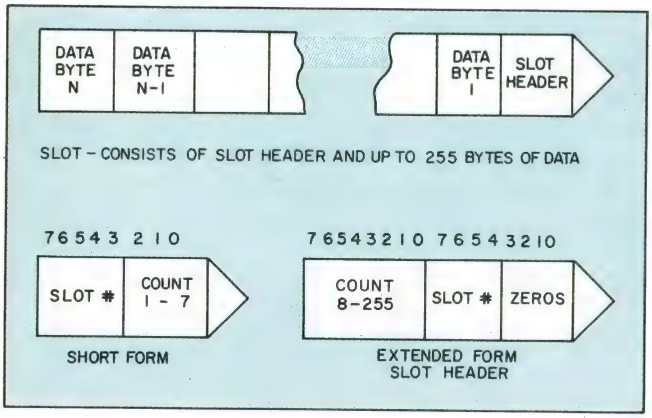
2. The data subfield of an information frame contains as many as eight groups. Each of these groups, in turn, contains up to 31 distinct time slots.

flags and abort sequences, and appends flags. Only correctly received frames are passed to the next layer. Line-layer functions at the line-network interface are performed by an LSI—Motorola's 6854 Advanced Data Link Control device.

ARQ layer recovers from errors

While the Line layer detects errors, the ARQ layer performs error recovery. The ARQ layer supports balanced and extended-balanced transmission modes and provides two-way simultaneous (full-duplex) communication with continuous framing, which is a specific application of the general X.25 recommendation.

Within this second layer, two fields specify address and control functions. The address field, containing 8 bits, corresponds to a local or remote, A-unit or B-unit, address. Depending on the time needed to initialize a link, the control field contains either 8 bits in the normal mode or 16 bits in the extended mode.



3. The header in each of the 31 time slots contains the slot number and a count of the number of data characters going to the port addressed by the slot number.

The normal mode can support up to seven unacknowledged frames and is intended for systems with short delay relative to the data rate. For transmission systems with long delay, the extended mode supports up to 127 unacknowledged frames.

The use of either the normal 8-bit or extended 16-bit control fields in the MPP constitutes an extension of X.25 Level 2.

The ARQ-layer control field specifies one of three frame types:

- An unnumbered frame for link control
- A supervisory frame (S) for overseeing link operation; it carries retransmission requests
- An information frame (I) for user data.

When an I frame is passed from the Line layer to the ARQ layer, the frame sequence number, in the control field, is compared to a receive state variable maintained in the ARQ layer. This variable defines the sequence number of the next frame that is expected. If the two numbers match, the frame is processed and the receive state variable is incremented. If the two numbers do not match, the frame just received is out of sequence—as happens when an erroneous frame is previously received and discarded by the line layer.

To recover the lost frame or frames, the receiver issues a reject response requesting retransmission. The ACK sequence number in a supervisory-type frame specifies the number of the frame that had not been received by the ARQ layer. Starting with the frame identified by the ACK sequence number, the transmitter retransmits the approximate frames from its retransmission queue. Frames with a sequence number smaller than the ACK sequence number are acknowledged and flushed from the queue.

In an I-type frame, the ACK sequence number indicates the sequence number of the next expected frame and acknowledges the correct reception of frames with a lower sequence number.

Error protection, under MPP, not only operates unidirectionally, as described, but also in a full-duplex, Go-Back-N ARQ mode.

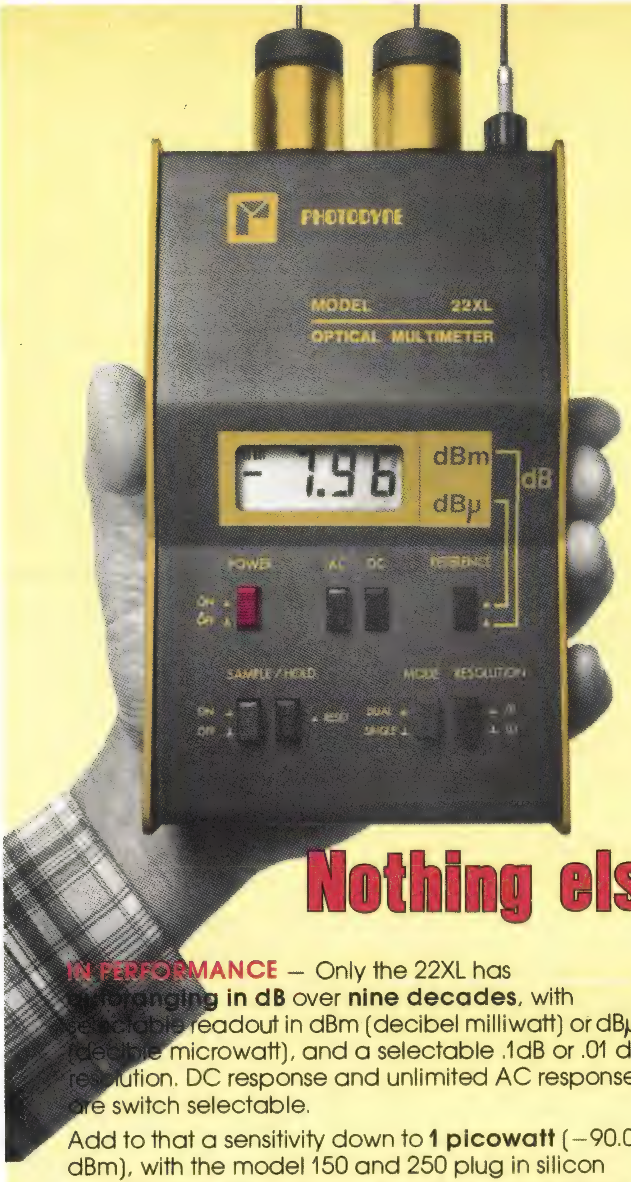
The inner layers of the MPP deviate from their X.25 counterparts. The third or Multiplex layer processes the I field, which contains two subfields: one for control information, the other for data. A control-byte flags the presence of control information. Additionally, a command code identifies the class or type of control information present: report messages, port-configuration parameters or statistical information.

The data subfield (Fig. 2) contains as many as eight groups, each containing up to 31 time slots. Fig. 3 details each slot. The header defines the slot number and a count. The slot number corresponds to the address of a physical terminal port; and the count specifies the number of data characters present that are associated with that terminal.

Data are transmitted in accordance with the Connection layer of the innermost protocol. Coded bytes are prefixed with a unique escape character, so that port-level control information, such as control signal updates, can be passed within the data stream.

The frames transmitted between network nodes vary in length because of frame changes and variations in the length of the I frame or data field under changing traffic patterns. For terminals that do have data to transmit, port addresses are supplied along with the number of data bytes in the frame. Because no time slot is allocated to it, an inactive terminal (no data to transmit) is automatically dropped from the frame. An obvious improvement in line efficiency results. This technique of concentrating asynchronous data stream provides three benefits: The data are protected from errors, line-use efficiency goes up and the transmission is transparent.■■

How useful?	**Circle No.**
Immediate design application	**544**
Within the next year	**545**
Not applicable	**546**



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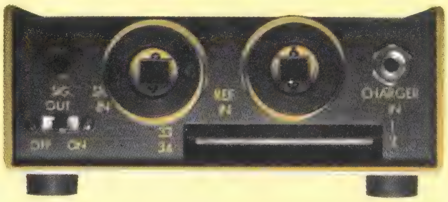

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CIRCLE NUMBER 51

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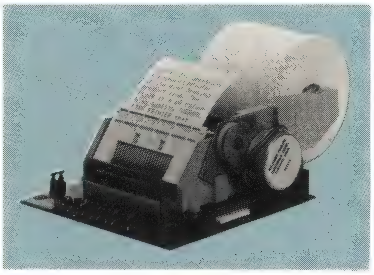

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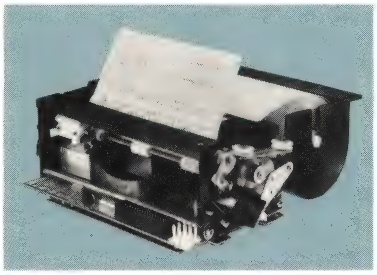

- Microprocessor controlled thermal printer
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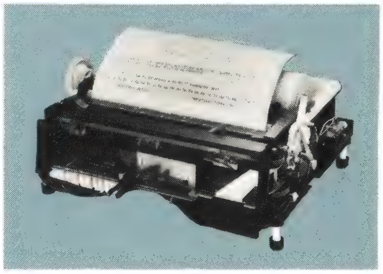

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- Standard 96 character ASCII set plus external character generator
- Throughput rate — 30 characters per second
- Signalling rates
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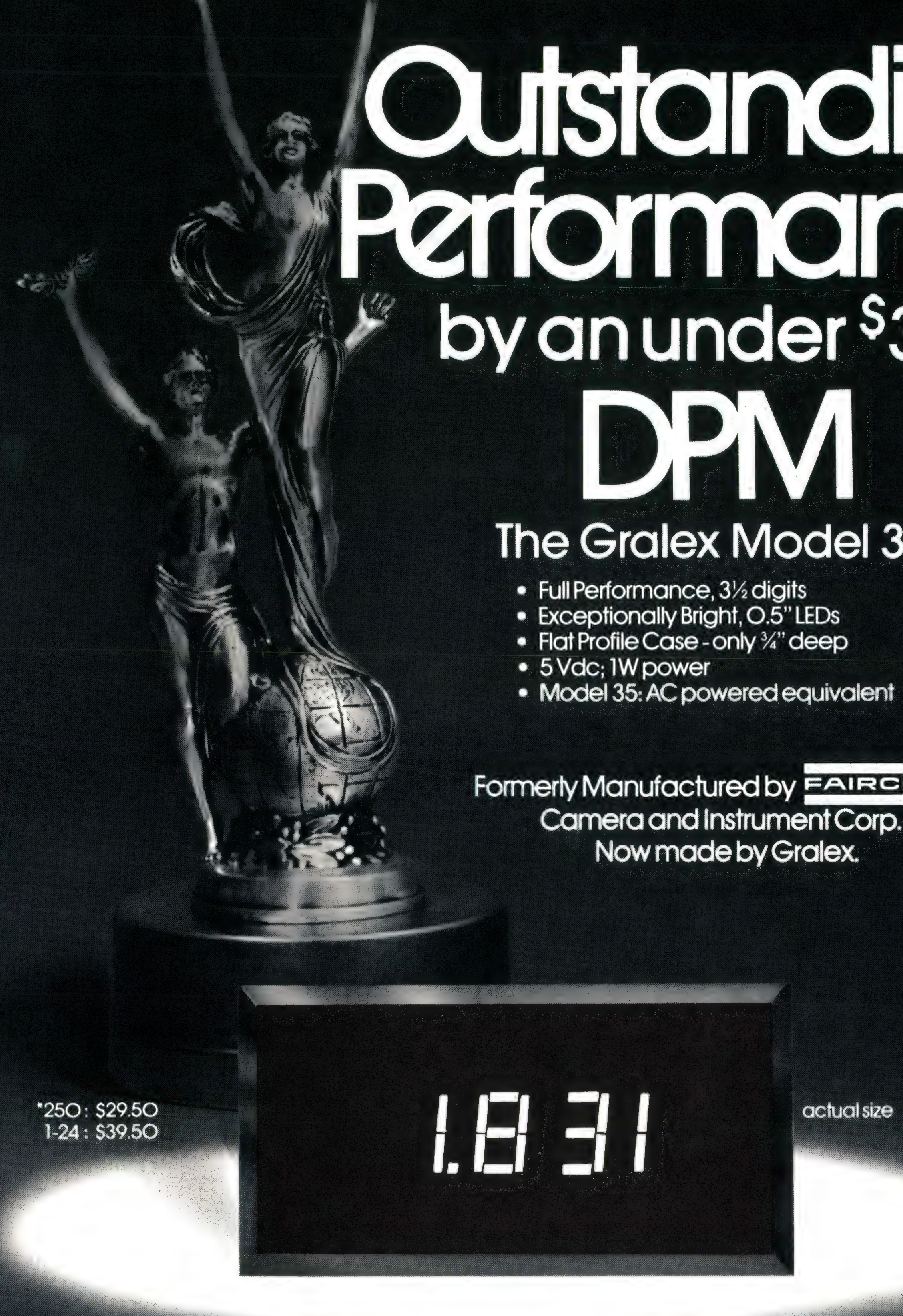
CIRCLE NUMBER 58



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CIRCLE NUMBER 52

A different approach to subroutine calls can save program space for Cosmac μPs

Users of Cosmac μPs who often call nested subroutines would do well to look at an alternative to the three subroutine-organizing techniques in the RCA user's manual.[1] Depending on specific requirements, a fourth approach, the stack-subroutine technique (SST), can often save program space.

Before looking at SST in detail, it would be worthwhile to summarize the techniques, advantages and disadvantages of the three standard methods.

SEP register is the simplest technique. It requires six bytes in the main routine for initialization of the subroutine register, and one byte for each call. Each subroutine needs three bytes (in addition to the subroutine codes) to ensure that the subroutine register will again point to the subroutine entry point when subroutine execution is complete. The total overhead, in bytes, is

$$N_{SEP} = 6 + 1 \times C + 3 = 9 + C,$$

where C is the number of calls to the subroutine. But SEP has one big disadvantage—it cannot call other subroutines.

The MARK technique requires six bytes to initialize the subroutine register with its entry point, five bytes to guard the contents of the subroutine register and to return to the main program, and three bytes for each call. This adds up to

$$N_{MARK} = 6 + 3 \times C + 5 = 11 + 3\,C.$$

Unlike SEP, MARK can call other subroutines.

The SCRT approach requires 18 bytes to initialize the three registers that contain the entry points of the subroutines CALL and RETPGM, and the stack pointer. Three more bytes are needed each time the subroutine is called and 29 bytes are used for CALL and RETPGM. In the subroutine itself, only one additional byte is needed. The total number of overhead bytes is therefore:

$$N_{SCRT} = 18 + 3 \times C + 29 + 1 = 48 + 3\,C.$$

But since 47 bytes are common to all SCRT subroutines, the overhead per subroutine becomes

$$N_{SCRT} = 1 + \frac{47}{S} + 3\,C,$$

where S is the number of subroutines using SCRT.

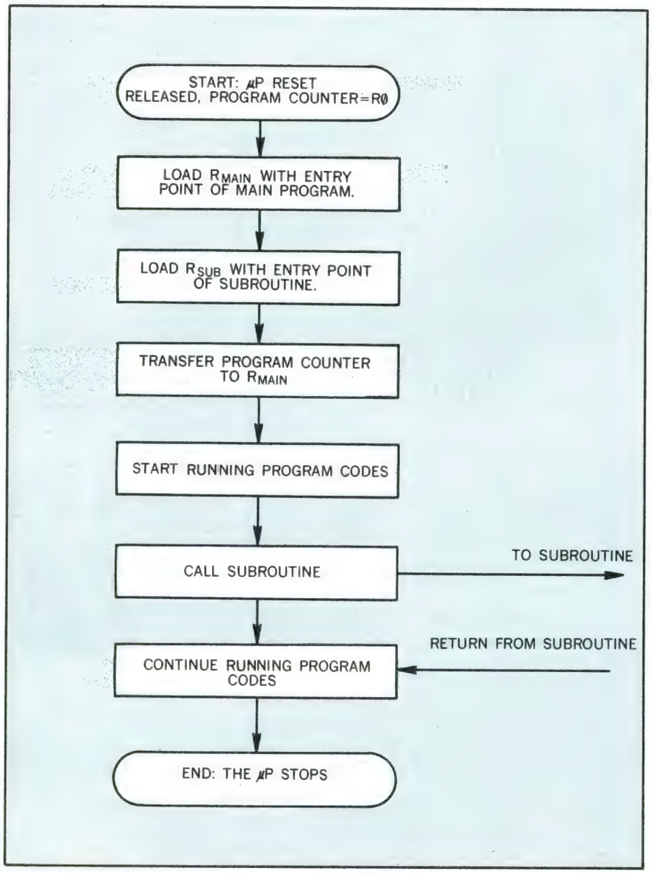
Oded Yossif Or, Senior Electronics Engineer, Tadiran, Israel Electronics Industries Ltd., P.O. Box 276, Holon, Israel.

The main advantage of SCRT is that a new subroutine, once included in the program, does not require an added register. For an additional SCRT subroutine, the value of N is only

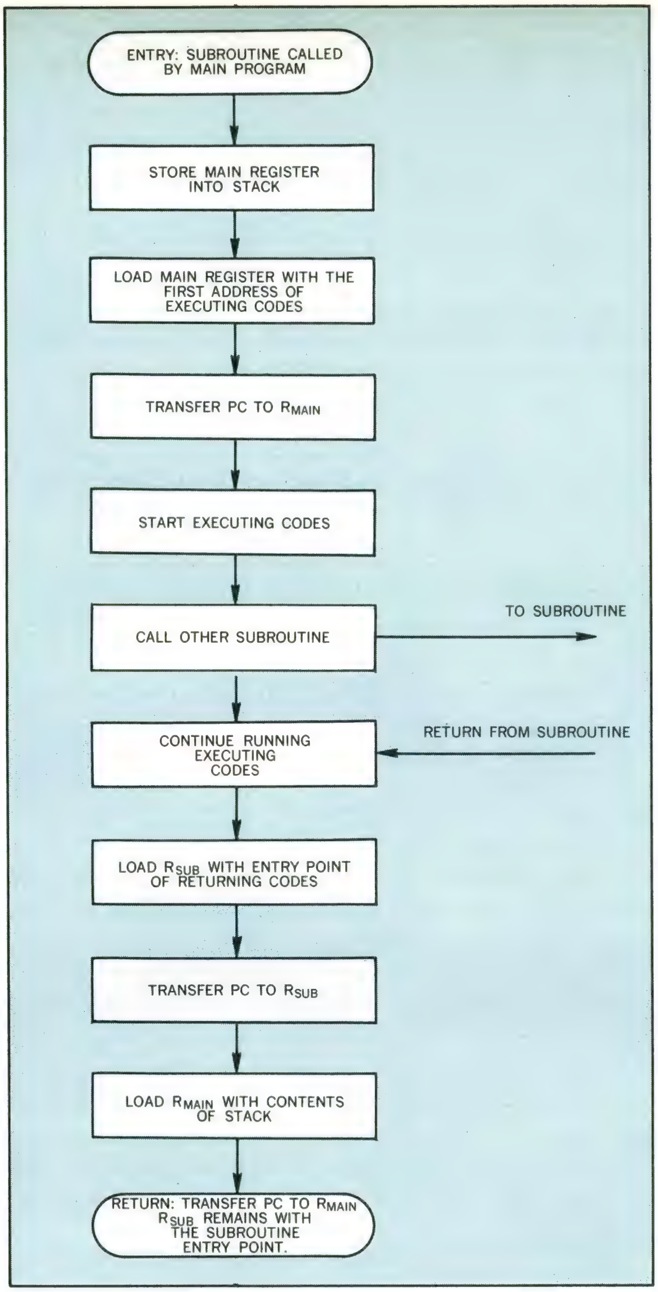
$$N_{SCRT}{}^{*} = 1 + 3C.$$

Bigger can be smaller

The new SST approach uses a stack without a stack pointer. Although it needs at least 25 bytes, it often saves programming space. With it, a subroutine can be accessed by using only one byte whose address is stored in a specific stack. After subroutine execution the μP returns to the calling routine, leaving the subroutine entry point in the subroutine register just as it does during program initialization. To use SST,


START: μP RESET RELEASED, PROGRAM COUNTER=R0
LOAD RMAIN WITH ENTRY POINT OF MAIN PROGRAM.
LOAD RSUB WITH ENTRY POINT OF SUBROUTINE.
TRANSFER PROGRAM COUNTER TO RMAIN
START RUNNING PROGRAM CODES
CALL SUBROUTINE
TO SUBROUTINE
RETURN FROM SUBROUTINE
CONTINUE RUNNING PROGRAM CODES
END: THE μP STOPS

1. The main-program flow chart for SST (stack subroutine technique) shows the preparation of two registers—R_{main} and R_{sub}. White blocks are inserted as often as needed.


ENTRY: SUBROUTINE CALLED BY MAIN PROGRAM
STORE MAIN REGISTER INTO STACK
LOAD MAIN REGISTER WITH THE FIRST ADDRESS OF EXECUTING CODES
TRANSFER PC TO R_{MAIN}
START EXECUTING CODES
CALL OTHER SUBROUTINE
TO SUBROUTINE
CONTINUE RUNNING EXECUTING CODES
RETURN FROM SUBROUTINE
LOAD R_{SUB} WITH ENTRY POINT OF RETURNING CODES
TRANSFER PC TO R_{SUB}
LOAD R_{MAIN} WITH CONTENTS OF STACK
RETURN: TRANSFER PC TO R_{MAIN} R_{SUB} REMAINS WITH THE SUBROUTINE ENTRY POINT.

2. The subroutine flowchart for SST code helps explain the program listing in Fig. 3. White blocks are inserted as often as needed.

```
INIT:  LDI  A.1        (Main)

       PHI  RMAIN
       LDI  A.O.   (Main)...    Load   RMAIN
       PLO  RMAIN.............. with  AMAIN
       LDI  A.1        (SUB)
       PHI  RSUB


       LDI  A.0   (SUB).....    Load   RSUB
       PLO  RSUB................ with  ASUB
       SEP  RMAIN.......... Jump to MAIN
            ......... With PC=RMAIN
MAIN:  .
       .
       SEP  RSUB........... Call subroutine
       .
       .

       SEP  RSUB 2............ Call another
                                 subroutine
       .
       .

       SEP  RSUB........... Call subroutine
       .
       .
       .
```

```
EXIT:  GHI  RSTACK........... Return the
                          calling routine
       PHI  RMAIN.. PROGRAM COUNTER
       GLO  RSTACK............. from the
       PLO  RMAIN.................. stack
       SEP  RMAIN...... Return to RMAIN
            .......... and continue
            ......... with the main
            ............... program
START: GHI  RMAIN.......... Store calling
       PHI  RSTACK........... routine PS
       GLO  RMAIN............. into stack
       PLO  RSTACK
       GHI  RSUB
       PHI  RMAIN
       LDI  A.0        (SR)
       PLO  RMAIN........... Change the
       SEP  RMAIN..... Program Counter
            ............... to RMAIN
SR:    .

       .
       SEP  RSUB 2.......... Call another
                             subroutine
       .

       .
       LDI  EXIT........... Jump to EXIT
       PLO  RSUB......... With PC=RSUB
```

3. Main-program and subroutine code for the SST approach shows how the 25 overhead bytes are used. For the call itself, only one byte is needed.

however, the following provisions must be included in the program:

- To prevent erasure of the calling-routine stack, stack subroutines should be arranged by nesting level, so that each subroutine can only call one from a higher level. In addition, a specific stack must be reserved for each subroutine level.
- The main program should allocate a specific register (R_{SUB}) for the subroutine, start the main routine by loading the subroutine register with the entry point of the subroutine, and call the subroutine from the main program (or from a lower-level subroutine) when required via the command SEP R_{SUB}.

Then come the following steps in the stack subroutine:

1. Store the contents of the main-program counter in the stack at the subroutine entry point.
2. Use the same counter for the subroutine and the main program.
3. Continue executing the subroutine code, which may call higher-nesting-level subroutines.
4. Load R_{SUB} with an address five bytes below the subroutine entry point.
5. Change the program counter to the subroutine register and jump to an address five bytes below the entry point.
6. Load the main-program counter with the return address from the stack in the location five bytes below the stack subroutine entry point, using a SEP R_{MAIN} command, so that the SEP command will be stored just before the subroutine entry point. While this command is being executed, R_{SUB} again accepts the entry-point address.

The assembly code for the operation of an SST subroutine is given in Figs. 1 through 3; note that, once the registers are initialized, the program counter uses register R_{MAIN} and continues to operate on the main program. The subroutine can be called whenever needed. In the subroutines, the contents of R_{MAIN} are first stored in the subroutine stack so that the program counter can use R_{MAIN}. The execution codes are run and other subroutines are called if required. The program counter then jumps back to R_{SUB}, and the return address to the calling subroutine is transferred back from the stack into R_{MAIN}. The program counter then returns to R_{MAIN} via a SEP R_{MAIN} command. Because this command is in the last address before the entry point, R_{SUB} does not change during program initialization.

With six bytes needed for register initialization, ten for START, nine for EXIT, and just one for a CALL, the total becomes

$$N_{SST} = 25 + C.$$

Is it worth the trouble?

To see whether SST is justified, consider how well it can be integrated into existing techniques. First, review the number of additional bytes required by each technique:

Case	Conditions				Optimum technique	
	Register available?	SCRT used elsewhere?*	Nesting required?	C_c†	$C<C_c$	$C>C_c$
1	NO	¶	¶	—	SCRT	SCRT
2	YES	NO	NO	—	SEP	SEP
3	YES	NO	YES	7	MARK	SST
4	YES	YES	NO	4	SCRT	SEP
5	YES	YES	YES	12	SCRT	SST

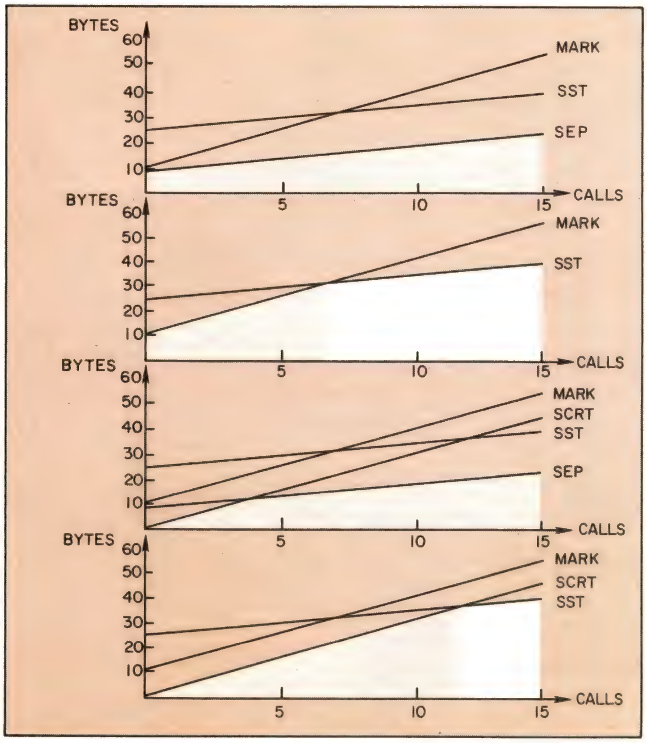
* If SCRT has already been used for another subroutine, the CALL and RETPGM routines have already been written.
¶ C_c is the critical call number (see Fig. 3).
† SCRT is the only choice—whether SCRT is available or nesting required.

4. The subroutine technique to be used depends on several factors: Availability of registers, nesting and number of subroutine calls in a given program are most important for using SST.

Subroutine technique	No. of added bytes
SEP REGISTER	$9 + C$
MARK	$11 + 3C$
SST	$25 + C$
SCRT	$1 + \frac{47}{S} + 3C$

Now see whether sufficient registers are available for SST; if not SCRT must be used. If the registers are available, check whether SCRT might save bytes. Next, organize subroutines assuming that SCRT is not used in the program. Then, assume use of SCRT, and in the light of the following questions (see column headings, Fig. 4):

1. Is a free register available for the subroutine?



5. The cases of Fig. 4 are shown in graphic form to indicate at what number of calls one technique becomes better than another. SST territory is highlighted.

2. Is SCRT used elsewhere in the program? If so, CALL and RETPGM are already in the program format.

3. Is nesting required?

If the answer to (1) is no, then SCRT must be used, since SCRT does not require a register for each subroutine (case 1 in Fig. 4).

If a register is available for the subroutine, then the technique listed as cases 2 through 5 in Fig. 4 should be used.

Case 2 represents the simplest; CALL and RETPGM are not available and nesting is not required, so use the SEP technique which takes only 9 + C bytes.

If nesting is required and CALL and RETPGM are not available (case 3 in Fig. 4) MARK will be the optimal technique for $C < 7$ while SST is preferred when $C > 7$ (Fig. 5).

For $C = 7$, $N_{MARK} = N_{SST}$ and either technique is justified, although SEP cannot be used when nesting is required. If nesting is not required and SCRT has already been used, SCRT will save bytes only when $C < 4$.

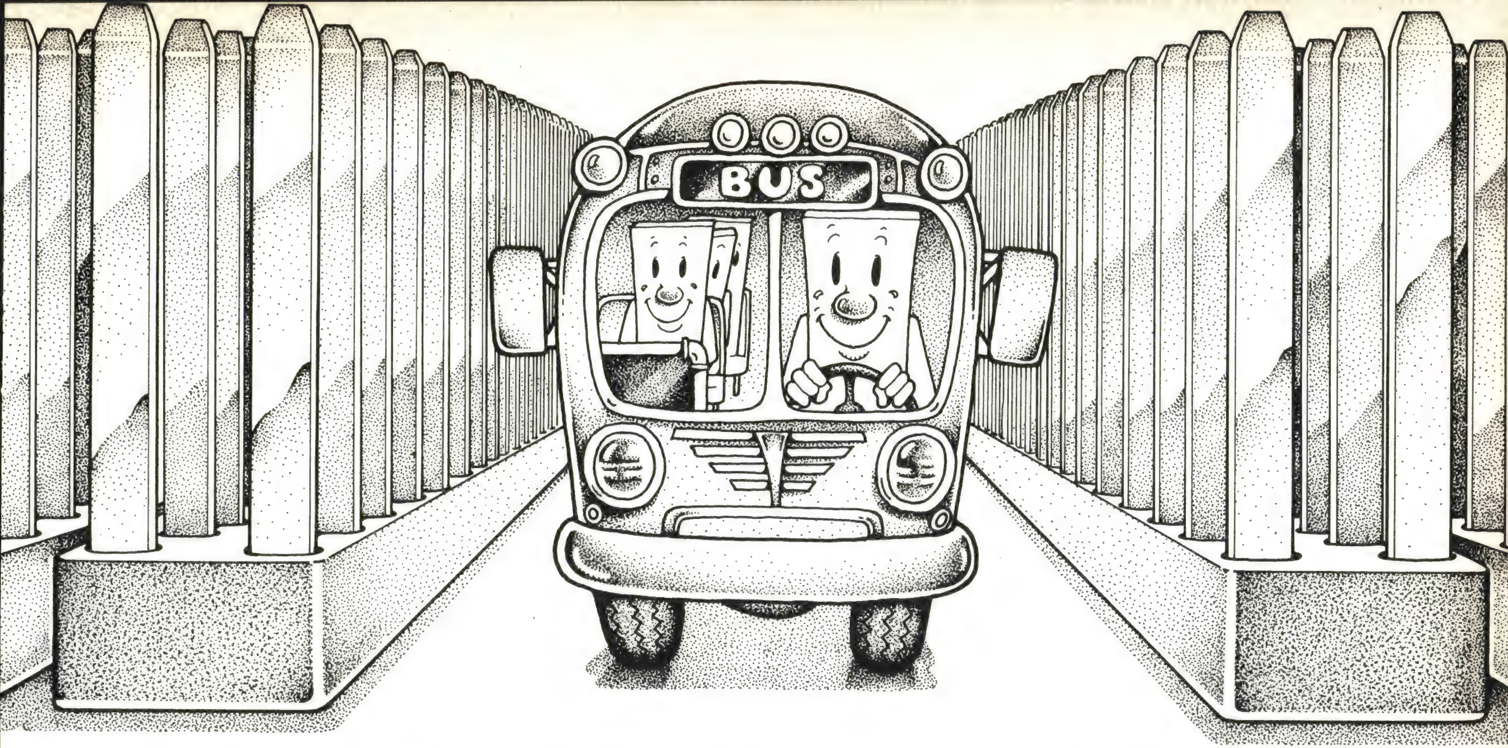
For $C > 4$, SEP is preferred (case 4). For $C = 4$, either technique is usable. But if SCRT is already used and nesting is required, look up case 5. When $C < 12$, SCRT is preferable, but when $C > 12$, SST has the edge.

If a particular subroutine is often called, SST is usually the best approach, provided the subroutine register is not otherwise needed. In Tadiran's HF/SSB transceivers, SST has proven to be highly efficient. In fact, as was found in designing VRC-476, when providing a SEP-subroutine with nesting, only SST allows the subroutine to be changed without affecting the calls to it.■■

Reference

1. RCA, "User Manual of Cosmac Microprocessor," MPM 201A 1976, pp. 54-64.

How useful?	**Circle No.**
Immediate design application	**556**
Within the next year	**557**
Not applicable	**558**



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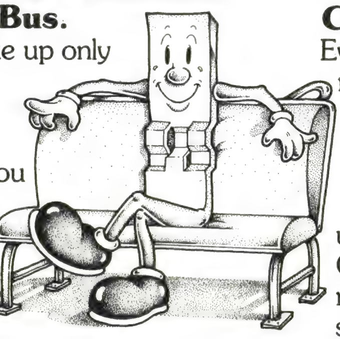

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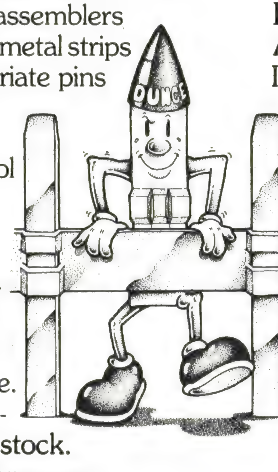

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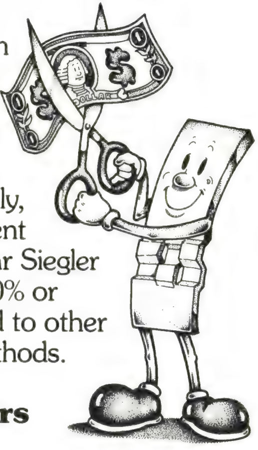

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LEAR SIEGLER, INC.
ELECTRONIC INSTRUMENTATION
DIVISION

CIRCLE NUMBER 109

Rate limit sensor ignores transients; works without large capacitors

The CA3080 operational transconductance amplifier may be used with the TL084 quad op-amp as a rate-limit sensor to monitor the time-rate-of-change of analog voltages. This circuit provides good immunity to small-amplitude, fast transients and, unlike conventional differentiators, does not need large capacitors to work with analog voltage rates-of-change that are relatively slow. The circuit provides an output only when the rate-of-change is greater than a preset amount. Often, this information is more important than knowing the rate itself.

Configured as a sample-and-hold amplifier, the CA3080 (A2), is strobed into operation periodically by system-derived pulses. (Most automotive and industrial control systems contain a clock output which may be divided, time-truncated and level-shifted, as necessary.)

Let V(t) be the analog voltage representing the monitored parameter; and let it vary between −7.5 and +7.5 V (see Fig.). During the strobe time, A2 transfers 1/3 $V(t_0)$ from its input to its output. When the strobe returns to zero, A2 reverts to a state of high-input impedance/high-output impedance, thus holding 1/3 $V(t_0)$ at pin 3 of comparator A3 and at pin 6 of comparator A4.

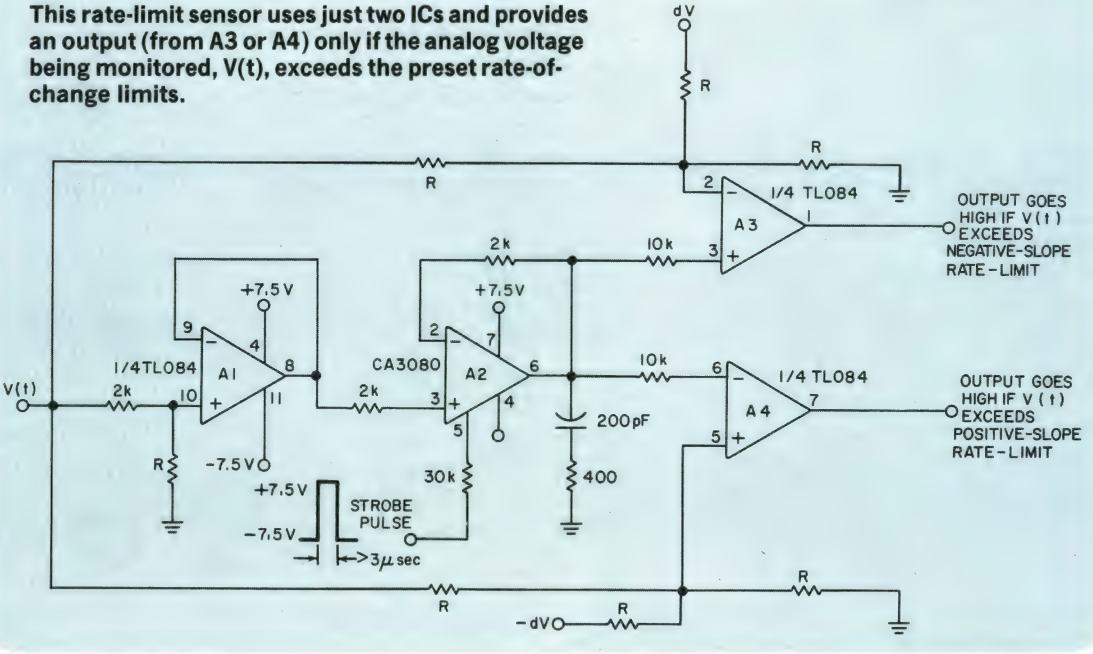
At pin 2 of A3, the voltage 1/3 [V(t) + dV] is presented. If $V(t_0) > V(t) + dV$, then V(t) has exceeded the negative-slope rate-limit and A3's output will go high. Comparator A4 provides a similar function for the positive-slope rate-limit.

The desired rate limits, together with the strobe rate, determine the values for +dV and −dV. Therefore, if T is the time between strobe pulses and if A is the rate limit, then dV must equal AT. The differential voltages, +dV and −dV, may be obtained readily, through appropriate resistor-divider networks, from the system's positive supply and negative supply, respectively.

Good noise immunity is provided so long as small, fast transients do not mimic the conditions specified by the inequality: $V(t_0) > V(t) + dV$. Noise immunity decreases as V(t) approaches $V(t_0) \pm dV$.

John Cyril P. Hanisko, Project Engineer, Bendix Advanced Products Div., 900 W. Maple Rd., Troy, MI 48084.

CIRCLE NO. 311



This rate-limit sensor uses just two ICs and provides an output (from A3 or A4) only if the analog voltage being monitored, V(t), exceeds the preset rate-of-change limits.

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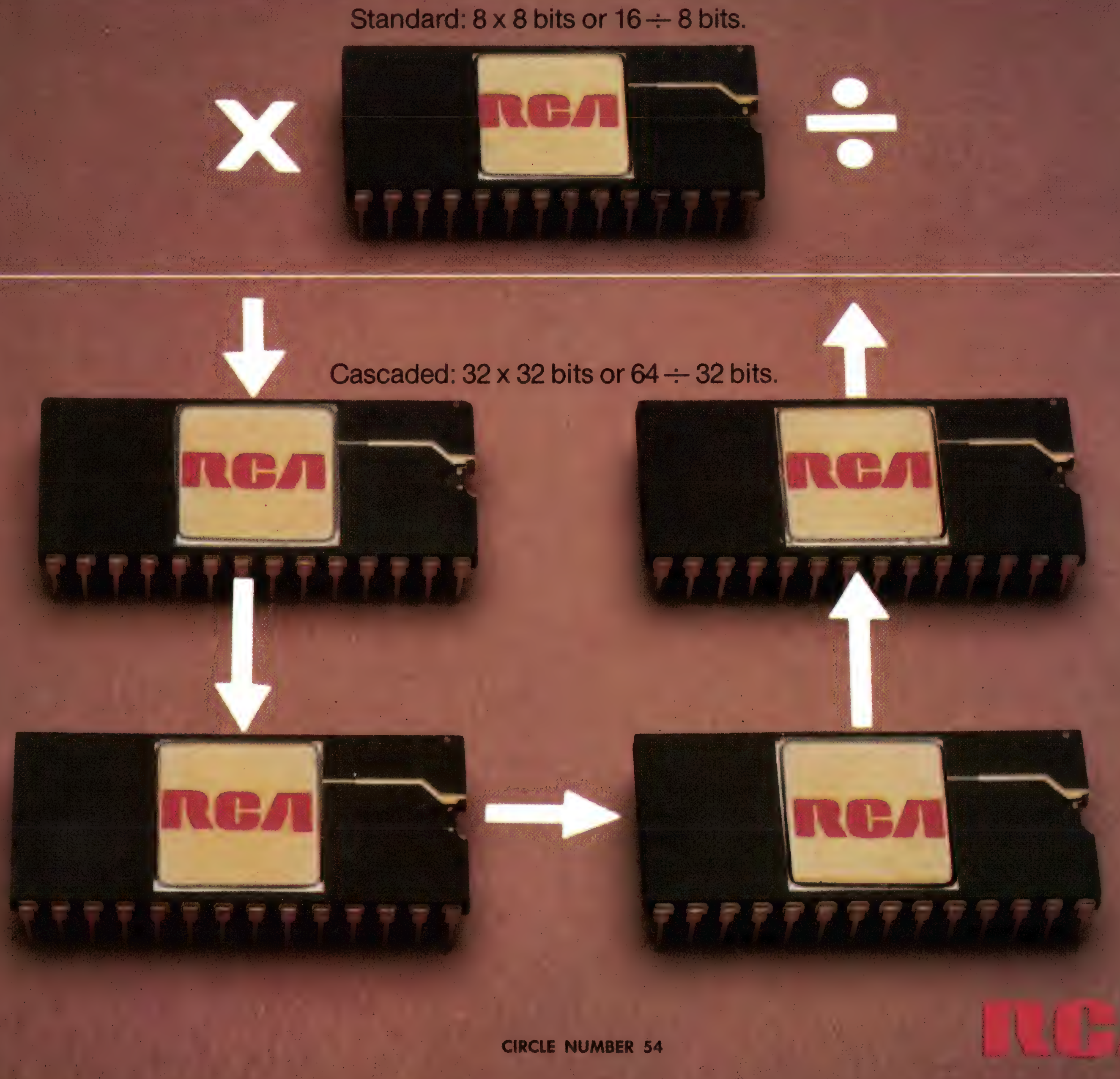
Standard: 8 x 8 bits or 16 ÷ 8 bits.
×
÷
RCA
Cascaded: 32 x 32 bits or 64 ÷ 32 bits.
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CIRCLE NUMBER 54

RCA

Bar-graph chip lights LEDs in series; minimizes current drain for displays

Solid-state bar-graph displays for consumer stereos and other electronic equipment typically contain ten LEDs driven in parallel. However, a series connection employing the LM3914 bar-graph driver can cut current drain by more than 80%.

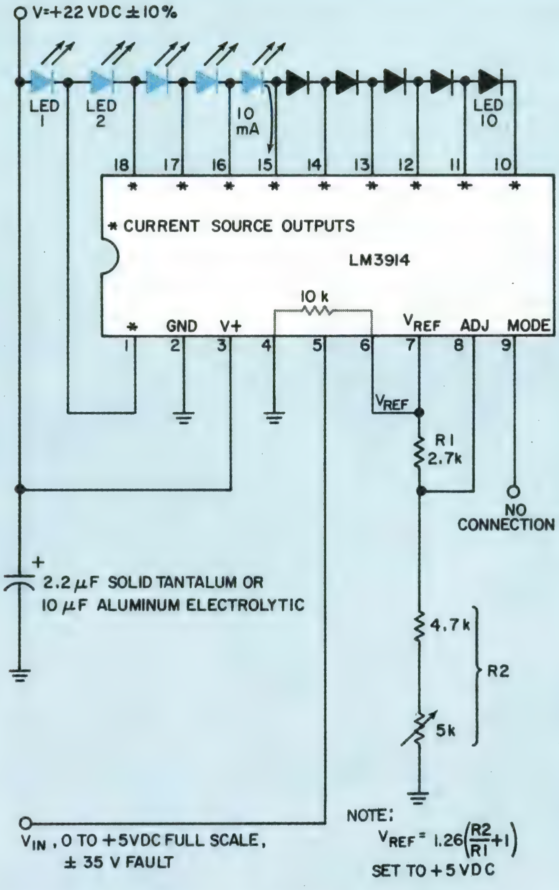
Normally, each LED draws 10 mA, for a potential current drain of 100 mA when all ten LEDs are on together. Should several simultaneous bar-graph displays be required, a drain of several hundred milliamps could easily develop. The LM3914 bar-graph driver chip can control up to ten LEDs in series with just 10 mA; it draws just 5 mA for itself.

This low current drain is possible because the LM3914 can work in either a conventional "bar" mode (supplying parallel currents) or in a "dot" mode (one current source on at a time). The LM3914 is in the dot mode when pin 9 is left unconnected (see Fig.). For scaling purposes, a 5-V reference voltage is connected to pin 6. Therefore, the LM3914 gives a "full-scale" reading when V_{IN} is +5 V or greater.

If V_{IN} lies below +0.5 V, no LEDs will be on. When V_{IN} lies between +0.5 and +1.0 V, 10 mA flows out of pin 1 and turns on LED 1. Every time the input voltage increases by 0.5 V, the 10 mA "shifts" to the next output pin, lighting an additional LED. For example, should V_{IN} increase to between +1.0 and +1.5 V dc, the current source at pin 1 will turn off and 10 mA will flow from the current source at pin 18, turning on LEDs 1 and 2 in series. When V_{IN} is +5 V or more (to a maximum of +35 V), all ten LEDs light in series, with the same 10 mA. Power dissipation will be primarily in the LEDs.

When V_{IN} is low and only one or two LEDs are on, the dissipation in the LM3914 is approximately 300 mW, and its case temperature is about 34 C above ambient. This combination does not exceed the ratings; but, for ambient temperatures above 60 C, it is advisable to glue a heat sink to the LM3914's dip package.

Most ordinary red LEDs have a forward voltage drop around 1.6 V (2.0 V worst case) at 10 mA. But for yellow, green or high-efficiency red LEDs, a 2.1-V drop at 10 mA is more likely. These LEDs can be accommodated only if V^+ is 24 V (regulated), instead of the 22 V shown.



The ten current sources within the LM3914 bar-graph chip are individually turned on and off by the amplitude of V_{IN}. Since only one current source may be on at a time in the "dot" mode, 10 mA may be routed through any series combination of up to ten LEDs. Here, five LEDs are on, indicating that V_{IN} is between 2.5 and 3.0 V.

Robert A. Pease, Staff Scientist, National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051.

CIRCLE NO. 312

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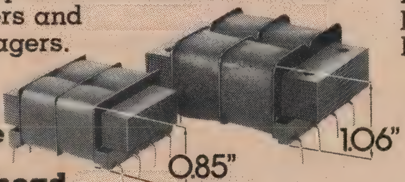

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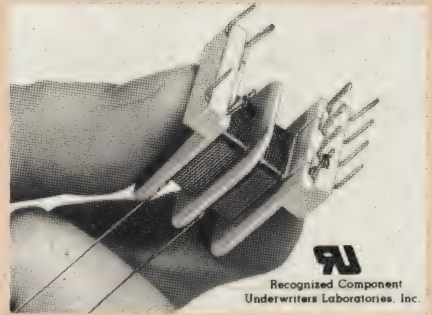

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TRANSFORMER

CIRCLE NUMBER 55

Counter and DAC replace analog integrator in delta-modulation scheme

A delta-modulated signal can be generated by combining an up-down counter with a digital-to-analog converter. The combination replaces an analog integrator and the counter provides a digital (sign and magnitude) output for applications such as pulse code modulation.

In the circuit (see Fig.), the output of the DAC is compared to the analog signal to determine the direction in which clock pulses will step the counter. If the comparator output is low, the counter counts up, until the DAC output exceeds the analog input. At this point, the counter reverses direction. In general, this process makes the DAC output track the analog input.

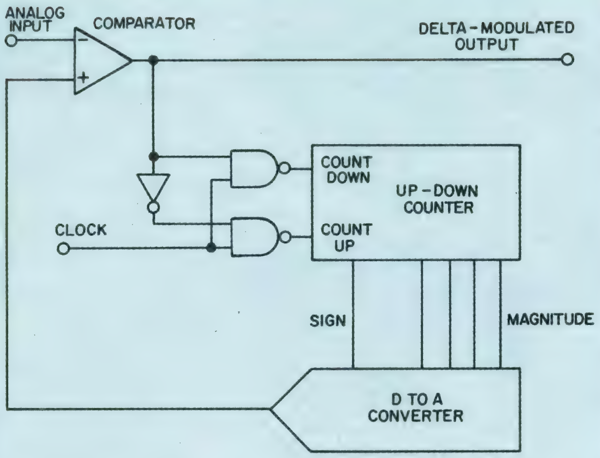
The delta-modulated signal comes from the comparator output. This signal can be demodulated at the receiving end by an up-down counter driving a DAC. The modulator and demodulator clock rates need not be identical. If they differ, the only parameter affected is voltage gain between the transmitter input and the receiver output.

At the receiver, the initial value in the counter offsets the dc level of the incoming signal. This offset can be eliminated by various methods; one of the simplest is to use a large series coupling capacitor.

The sign-magnitude up-down counter can be a circuit like that described by Frazier in *Electronics*, Nov. 9, 1978, p. 114.

N. Bhaskara Rao, Dept. of Electrical Engineering, UVCE, K. R. Circle, Bangalore 560 001, India.

CIRCLE NO. 313



Delta modulator without an analog integrator uses an up-down counter and DAC. The comparator's output determines the count direction, making the DAC output follow the analog input.

IFD Winner for September 27, 1979

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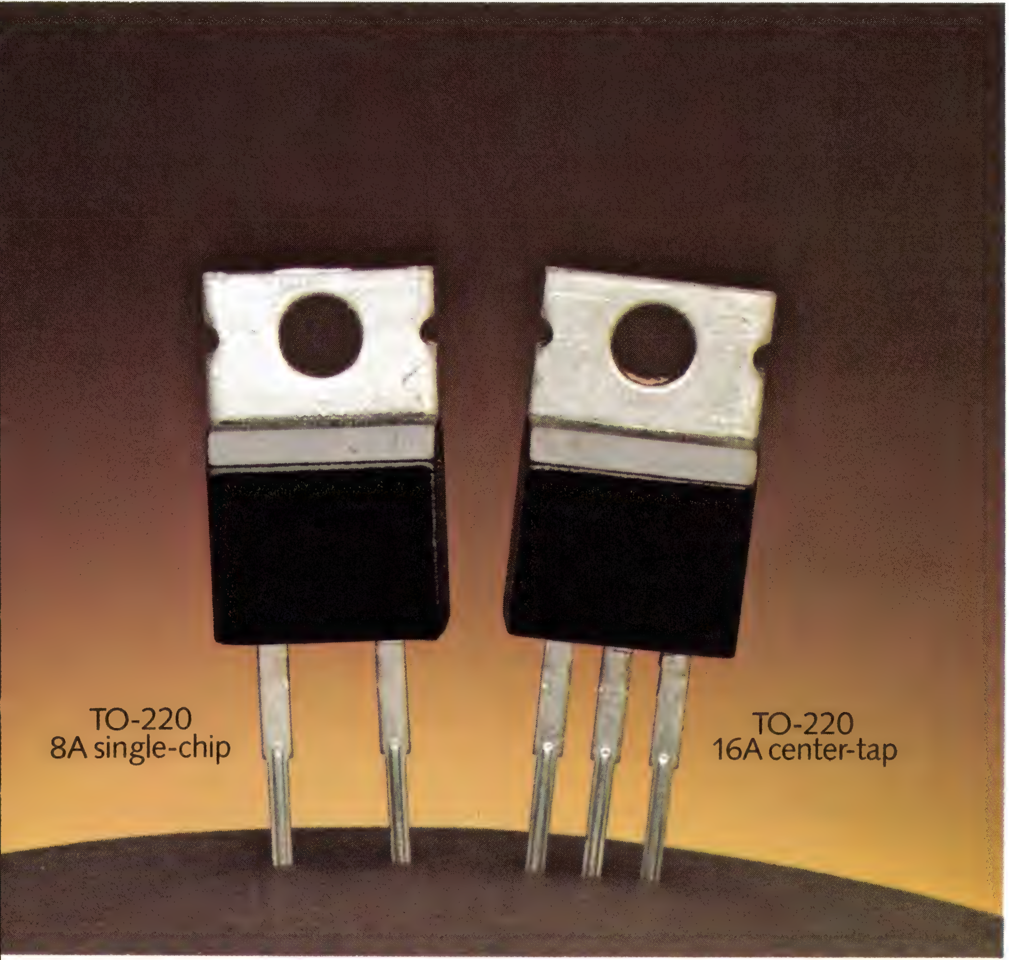

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CIRCLE NUMBER 135

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NEWS FROM PHILIPS

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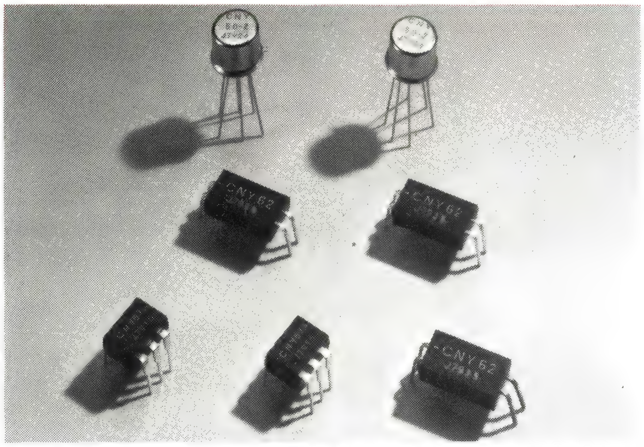
Designated the NFR series, the resistors are available in values 1 Ω to 15 kΩ (E24) with a 5% tolerance. The resistors comprise a homogeneous metal film deposited on a high grade ceramic body. Good contact reliability is assured by means of steel caps pressed onto the ends of the resistor body. Tinned electrolytic copper wires are welded to these caps. The resistors are coated with a grey flame retardant insulating lacquer. This lacquer is resistant against all commonly used cleaning solvents. Standard packaging is 1000 resistors per box, or 5000 per reel on bandoliers.

CIRCLE NUMBER 800



PROFESSIONAL PHOTOCOUPLERS

A number of new photocouplers have been developed for professional applications. Our CNY50 is a hermetically sealed photocoupler in a SOT-104B metal envelope for telephony and professional control applications. It consists of an infrared emitting GaAs diode and a silicon n-p-n photo-transistor with its base connection brought out.

There are two versions of the CNY50, differing only in their output/input d.c. current transfer ratios. The CNY50-1 has a value greater than 0,25 and the CNY50-2 has a value greater than 0,40 measured at a forward current of 10 mA and a collector emitter voltage of 0,4 V.

The maximum V_{CEO} of the photo-transistor is 35 V and the maximum forward current of the diode is 100 mA. Leakage current is less than 200 nA and the isolation voltage is 1 kV d.c.

To meet the highest safety requirements of VDE/DIN standards, a new series of photo-couplers has been developed. Four of the new types are the CNY52/53 and the CNY62/63. In the CNY52 and CNY53, the base connection of the silicon photo-transistor is brought out; the CNY62 and CNY63, which are otherwise identical, do not have this facility. The transistors of the CNY52 and CNY62 have a V_{CEO} of 50V maximum and the d.c. current transfer ratio is greater than 0,25. For the CNY53 and CNY63 these values are 30 V and 0,5. Insulation voltage for the CNY52 and CNY62 is 5,3 kV d.c. For the CNY53 and CNY63, the corresponding value is 4,3 kV d.c. These photocouplers are encapsulated in a SOT-91 plastic housing.

Two further types are the CNY57/57A. These are identical except for their current transfer ratio which is greater than 0,2 for the CNY57 and greater than 0,4 for the CNY57A. Transistor V_{CEO} is 30V maximum for these types and the insulation voltage is 4,3 kV d.c. The CNY57/57A are encapsulated in a 6-pin dual-in-line SOT-90 package.

CIRCLE NUMBER 801

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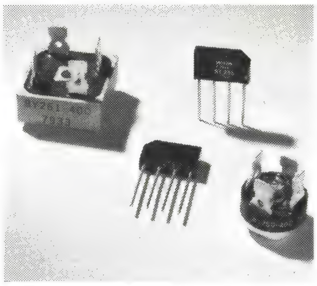
Our range of silicon full wave bridge rectifiers now extends from 1 A to 25 A output with the addition of four new types. These are the BY256, BY257, BY260 and BY261 series.

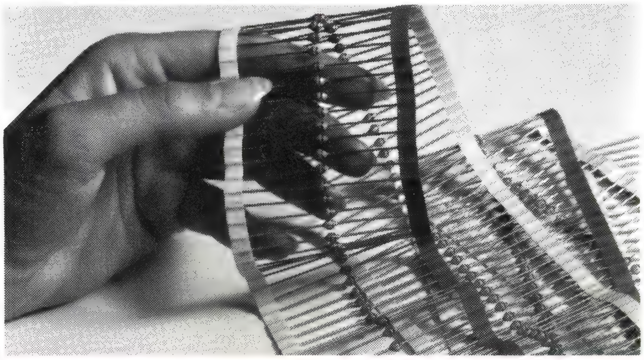
The first of these, the BY256, is a 1,5 A device ($I_{O(AV)}$), with a maximum input voltage rating of 80 V_{RMS}. It is suitable for use in equipment such as hi-fi amplifiers where an input mains transformer is employed. The BY257 is also a 1,5 A device, but has a maximum input voltage rating of 280 V_{RMS}. This type is particularly suitable for colour television receivers and in switched-mode power supplies up to 200 W.



The BY260 series and the BY261 series are intended for use as general purpose bridge rectifiers in industrial equipment. Each series consists of three versions having maximum r.m.s. input voltage ratings of 140 V, 280 V and 420 V, respectively. The BY260 has a maximum output current rating of 12 A, while the output current rating of the BY261 is 25 A.

CIRCLE NUMBER 802

GLASS BEAD RECTIFIER DIODES



Our new family of glass bead rectifier diodes is now becoming available in small quantities. Intended to take over the duties of existing plastic diodes, the new types feature extended voltage range, the same or faster switching speeds and higher current ratings. The diodes also have avalanche properties and are thus able to withstand reverse surges. The family currently comprises four new series: the BYV95, BYV96, BYW95 and BYW96. The BYV95 has three reverse voltage versions: the BYV95A for 200 V, the BYV95B for 400 V and the BYV95C for 600 V. Maximum forward current is 1,5 A and the reverse recovery time is less than 250 ns. The BYW95A, B and C are the equivalent 3 A versions; other ratings remain the same. The BYV96D and E are 800 V and 1000 V versions, respectively, of the BYV95A, B and C. Maximum forward current is again 1,5 A and the reverse recovery time is less than 300 ns.

The BYW96D and E are, likewise, the 800 V and 1000 V versions, respectively, of the BYW95A, B and C. Maximum forward current is 3A and the reverse recovery time is less than 300 ns.

CIRCLE NUMBER 803

Philips Industries
Electronic Components and
Materials Division
Eindhoven - The Netherlands

PHILIPS

Electronic
Components
and Materials

PHILIPS

Powerful 16-bit mini comes on a single PC board

Norsk Data A.S., P.O. Box 4, Lindeberg gard, Oslo 10, Norway. (02) 39 16 01.

Said to be the world's first high-performance single-board minicomputer, the Nord-100 weilds the computing power of 16 boards—the number of boards required by the previous generation of Nord computers.

By using bit-slice technology, the mini's designers were able to pack all that capability into a single multilayer board, only 28 × 37 cm. At the same time, they increased capacity by 40%, with better reliability, faster repair and lower power consumption. The Nord-100 applications range from small dedicated tasks to large distributed multicomputer systems.

A maximum of 64 terminals can be connected to the Nord-100, and they can execute many tasks simultaneously by means of a common command language. Several units can be hooked up to form a large distributed system, which functions as one unit. The minicomputer addresses up to 32 Mbytes of physical memory, with an additional 2304 Mbytes on disk.

Available in various sizes and configurations, the Nord-100 is normally supplied assembled in a compact cabinet. The removable front panel is serviced by a microprocessor, which operates independently of the programs run in the machine. A digital clock on the panel is fed from a battery, in the event of power failure. After loss of power, the system automatically restarts, and the digital clock updates the computer's internal clock.

The operating system of the Nord-100 enhances the computer's versatility. Typical applications would include: real-time applications for externally controlled processes; time-sharing for program development; transaction processing for administrative applications; batch processing for periodical and low-priority tasks.

Even though the basic technology of the Nord-100 is brand new, the system is fully compatible with earlier 16-bit computers in the Nord series. Programs and data files can be transferred directly.

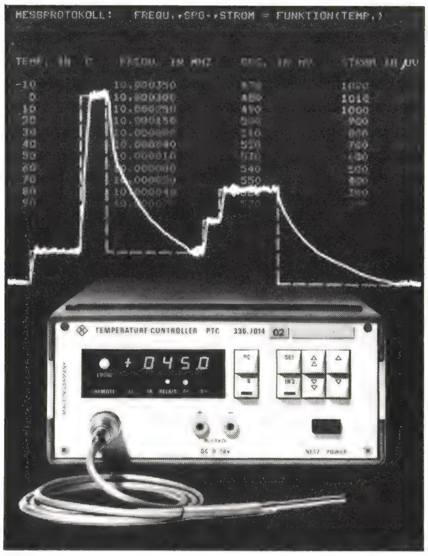
CIRCLE NO. 501

A first: Control temperatures over IEC bus

Rohde & Schwarz GmbH Pressestelle, Muhldorfstrasse 15, Postfach 801469, D-8000 Munich 80, Federal Republic of Germany. (089) 41292625. Telex: 523703.

The PTC temperature controller, with a built-in IEC-bus interface, is the first precision measuring and regulating system to be directly compatible with the IEC universal interface bus, an international standard.

The PTC allows temperatures from −100 to +300 C (173.2 to 573.2 K) to be precisely measured and controlled. Using a platinum resistance thermometer as the sensing element, it achieves an accuracy of 0.2°—with a resolution of 0.1°—throughout its entire temperature range. After the PTC compares the detected temperature value with a nominal value set by the operator, a control signal derived from this comparison switches a load relay—which can regulate a furnace or other loads. A built-in control relay allows direct connection to a climatic chamber.



A computer-based system can be built using the PTC controller, a furnace and IEC-bus compatible measuring instruments. Such a system could simultaneously control the temperature of the furnace, record the temperature and make other measurements. For example, the system could be used for environmental testing of electronic equipment.

CIRCLE NO. 502

Sweep generator phase-locks for stability

Texscan Corp., Export Div., 1 Northbridge Rd., Berkhampstead, Hertfordshire HP4 1EH, England. (44) 4427-6232. Telex: 82258.

The Model XR-1500 signal generator covers the frequency range of 1 to 1500 MHz in a single sweep. Because of its built-in phase-lock system, the instrument can also be used as a stable signal generator—the residual FM is only 1 kHz in this mode.

With its broadband coverage, the unit is extremely versatile. It can measure i-f and radio frequencies, for rf and vhf telecommunications and radar equipment. It covers all TV bands; and at the higher end of its range are TACAN, civil and military navigation and telemetry bands. Neither bandswitching nor band-edge glitches interfere with measurements because the XR-1500 does not use band stacking to achieve its broadband sweep.

Digital readout of center frequency is clearly displayed with 7-mm digits. Preset sweep width and other functions are selected by pushbutton switches strategically positioned for ease of operation. Lighted colors within the buttons identify various operations. The XR-1500 can sweep very-narrow-band circuits anywhere in the total frequency range of the instrument.

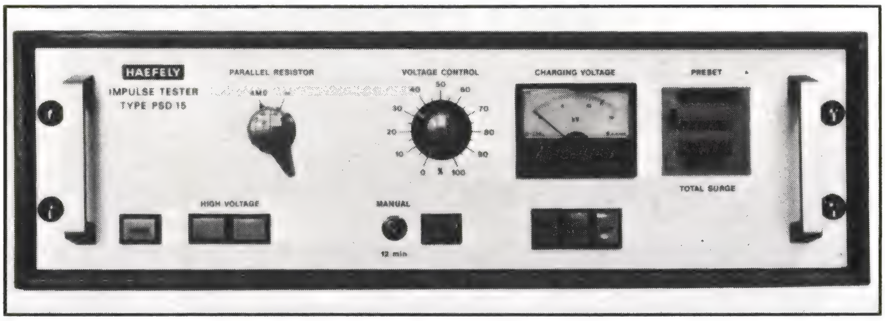
The phase-lock feature allows the XR-1500 to double as a stable signal generator: The residual fm of 1 kHz pk-pk is coupled with a stability better than 50 kHz for 5 min (after 1-h warm-up) in the phase-locked mode.

A built-in crystal marker system shows frequency with an accuracy of ±0.005%. The three-frequency calibrator shows birdies all the way to 1500 MHz. In addition to the built-in harmonic markers at 1, 10 and 100 MHz, there are provisions for another five plug-ins.

Exceptional flatness and precision built-in rf attenuation keep relative-amplitude measurements accurate to ±0.1 dB over narrow ranges and ±0.5 dB over the full 1500-MHz operating frequency range.

CIRCLE NO. 503

Make standard tests for static discharge



High Voltage Test Systems, Emil Haefely & Co. Ltd., Lehenmattstrasse 353, P.O. Box CH-4028, Basel, Switzerland. (061) 41 18 17.

A static-discharge simulator, the PSD 15, accurately and repeatably tests the effects of high voltage, low energy and transients on all types of equipment.

Today's MOS devices, especially high-density CMOS ICs, are extremely vulnerable to high voltage transients. Because the devices have high input impedances and tiny dimensions, the energy levels of the transients need not be very high to cause device failure.

Though design engineers have become increasingly aware of the static-discharge problem, and realize that they must take precautionary measures to combat it, no standardized measurements and few dedicated instruments are available to perform the tests. So the manufacturers of the PSD 15 will, within certain limits, adjust the characteristics of the simulator to conform with a customer's specific test requirements. The company will adjust the values of the impulse capacitance and discharge resistance, which determine the energy content and discharge rate of the simulated transient.

The basic PSD 15 allows the user to adjust the peak impulse voltage continuously from 0.5 to 15 kV. The nominal impulse capacitance is between 150 and 250 pF, while the discharge resistance is approximately 1.5 kΩ. With the standard component values, the stored energy is 125 μJ at 1 kV, 500 μJ at 2kV, and 12.5 mJ at 10 kV.

The user can release pulses manually by pushing a button, or set the simulator to generate pulses automatically at rates from 6/min to 60/min. Pushbuttons allow either positive or negative pulses to be generated. Pulse voltage can be accurately preset.

The tester is designed to operate from a 230-V, 50-Hz ac supply, and the sturdy unit can be conveniently mounted in a standard 19-in. rack.

CIRCLE NO. 504

Portable EPROM gang programmer is powerful but economical

Intertek Inc., 7-2-8 Nishi-Shinjuku, Shinjuku-ku, Tokyo, Japan 160. (03) 363-6649.

The PKMW-5000 compact gang programmer handles up to eight EPROMs simultaneously, with operation reportedly foolproof thanks to automatic self-checking features. Yet the programmer is relatively inexpensive. Supplied with four selection units, it costs 578,000 yen (FOB Japan).

With plug-in selectors, the PKMW-5000 programs virtually all the currently available NMOS EPROMs, including the 2516, 2704, 2708, 2758, 2716, 2732 and 2532. What's more, it weighs just 4.8 kg (10.6 lb), with power supply included, and measures 382 × 315 × 55 mm (15 × 12.4 × 2.2 in.).

Operation is simplified by automatic self-check functions such as a voltage-margin check, a check for shorts on address and data lines, a wrong-insertion detector, and a level limiter. A miniature speaker and 27 LED indicators confirm commands and inform the operator of the error status.

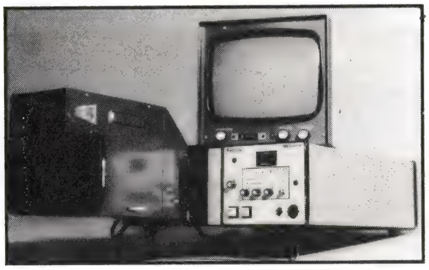
With intelligence coming from an internal Z80 microprocessor, Intertek designers were able to achieve powerful, foolproof performance without a substantial cost increase.

The power supply in the PKMW-5000 allows operation from various line voltages, including 100 V ac, 117 V ac, 220 V ac or 240 V ac ± 10%—from 50 or 60-Hz sources. Total power consumption is 60 VA. Operating temperature range is 4 to 40 C.

The PKMW is the second, and more advanced, of the Intertek Pecker series. The first in the series was the PKW-5000—more popularly known as the Pecker 1. The new unit is called the Pecker 8.

CIRCLE NO. 505

Oscilloscope video camera also takes Polaroid photos



Graphic Display Systems Ltd., 76 Hemingford Rd., Cambridge CB1 3BZ, England. Madingley (90954) 210486.

An oscilloscope-camera system, GDS-4000, combines a Polaroid camera and a video-imaging system in a single unit. The complete system forms a compact, pivot-hinging unit that joins a bezel adaptor to fit most oscilloscopes. Suitable for medical or lab use, the system lends itself to any situation requiring continuous video taping combined with instantaneous Polaroid "snapshots." The black-and-white system works with grey-scale displays or conventional oscilloscope traces. It can also be used with a suitable video display to provide instruction or demonstrations for remote or large audiences.

CIRCLE NO. 506

Wide-range thermometer reads Celsius or Fahrenheit

Noronix Ltd., 66-70 Bourne Rd., Bexley, Kent, England. (032 25) 56446

A compact digital thermometer, NTD 20C/F, measures temperatures from − 70 to +1200 C or −94 to +1999 F, and shows readings on either scale at the touch of a switch. Powered by a standard 9-V battery, the instrument is small enough to be held in one hand. To conserve power, advanced CMOS circuitry is used for linearizing, cold-junction and auto-zero drift correction. The LCD display shows 4-1/2 digits—the last one is "C" or "F." Accuracy on both scales is ±0.2% ±1°. The thermometer uses a standard K-type thermocouple.

CIRCLE NO. 507

Thermocouple connectors are subminiature units

Ancom Ltd., Devonshire St., Cheltenham, Gloucestershire GL50 3LT, England. (0242) 513861.

Subminiature thermocouple connectors—said to be the smallest available—are recommended for use with fine-gauge thermocouple wires and protection tubes, where standard-size connectors become unwieldy. The heavy-duty connectors are made from glass-filled nylon and are ANSI color-coded for ease of use—with body color indicating the type of thermocouple alloy. The male connector has a predrilled brass bushing to which a protection tube can be soldered or brazed, eliminating the need for tube clamps. Wires with diameters from 0.0005 to 0.02 in. can be used. A wide variety of suitable alloy types are available. Panel-adaptor clips allow the connectors to be mounted in control panels and instrument cases. Two types are available: one for a rectangular knockout and the other for a round hole.

CIRCLE NO. 508

International New Products

Pushbutton keypad has telephone layout

Wirsbo Elektronik AB, Ölandsgatan 42, S-11663 Stockholm, Sweden. (08) 743-0845.

A numeric pushbutton keypad, KTG-6200, conforms to the standard telephone arrangement and spacing. It is built from 12 WT-5G switches mounted on a printed-circuit board. The switch element is a new item in the manufacturer's range of mechanical gold-cross switches. Because the moving part of the switches is a double-shot molded plunger, loose keytops are not needed.

CIRCLE NO. 509

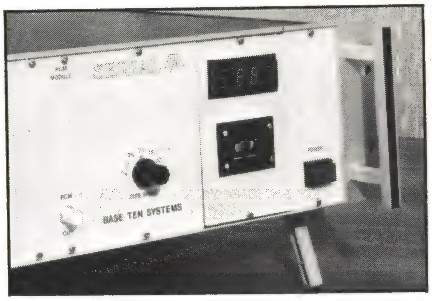
Peripheral units expand capabilities of teleprinter

The Exchange Telegraph Company Ltd., 73/75 Scrutton St., London EC2A 4PB, England. (01) 739-2041

Two add-on packages for the LA34 DECwriter IV extend the capabilities of the desktop teleprinter terminal. One package combines the DECwriter with Extel's RP-30 paper-tape punch/reader to provide full ASR (automatic send/receive) operation. The other package combines the terminal with the Extel 951 Microdisc to provide comprehensive data capture, storage, preparation and editing capabilities. Both add-on units are small, desktop devices. The RP-30 is a 30 char/s punch/reader with editing facilities. The 951 uses a miniature floppy disk to store over 200,000 characters.

CIRCLE NO. 510

Low-cost PCM decoder gives four analog outputs



Base Ten Systems Ltd., 12 Eelmoor Rd., Farnborough, Hampshire GU14 7QN, England. (0252) 517665. Telex: 858888.

A low- cost decommutator for pulse-code-modulation data signals, Serial 71, provides up to four analog signal outputs. The basic unit decodes a PCM data stream consisting of up to 16 multiplexed channels. Any one of the 16 decoded digital outputs can be selected for 4-digit numerical display. Simultaneously, the digital output can be fed, via a standard interface, to a PDP-11 minicomputer for subsequent data processing. Four of the 16 channels can also be selected as analog outputs. The decommutator accepts data streams using any of the following codes: NRZ (L, M, S), Bi-phase (L, M, S), or DM-M. Designed to decode PCM data with 8 to 12 bits per word and up to 16 words per frame—selectable by internal links—the Serial 71 accepts bit rates up to 50,000 samples per second. With a built-in 16-bit interface for the PDP-11, it costs £3950.

CIRCLE NO. 511

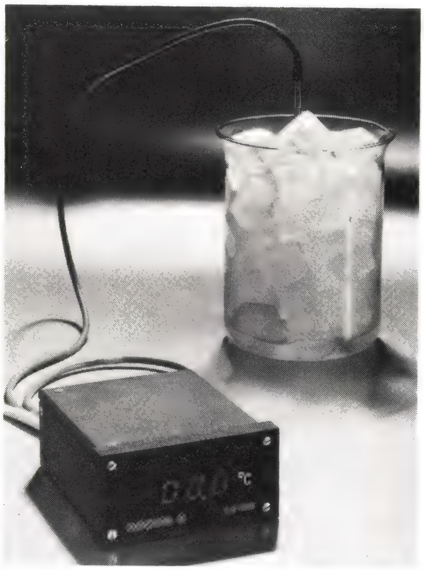
SAW devices provide pulse compression/expansion

Plessey Semiconductors Ltd., Cheney Manor, Swindon, Wiltshire SN2 2QW, England. (0793) 36251. Telex: 449637.

A matched pair of surface-acoustic-wave devices, SW8002 and SW8003, replace complex LC networks in pulse-radar applications. The pulse compressor (SW8002) and expander (SW8003) are designed for use in 60-MHz radar i-f subsystems. A growing number of military radars use pulse-compression techniques to increase range and sensitivity for a given peak power. The compressor/expanders generate FM waveforms and reprocess received waveforms. A chirp pulse with a bandwidth of 25 MHz and a duration of 2.2 μs, centered on 60 MHz, is produced by driving the expander with a fast impulse. After transmission the pulse can be compressed by the SW8003 to a 50-ns pulse, with a processing gain of 17 dB. The monolithic SAW devices are packaged in 16-pin DIPs for convenient PC-board mounting.

CIRCLE NO. 512

Digital thermometer has 0.1-degree resolution



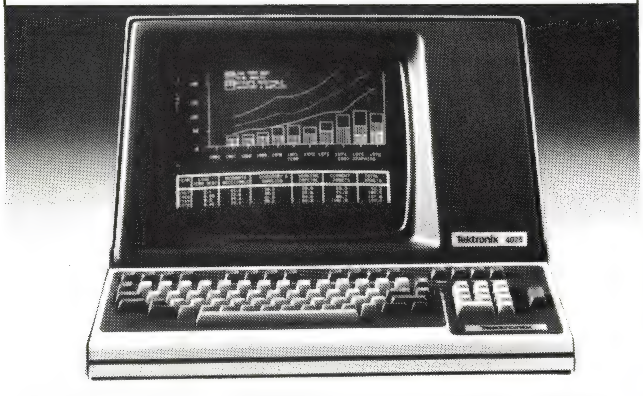
Ancom Ltd., Devonshire St., Cheltenham, Gloucestershire GL50 3LT, England. (0242) 53861 or 24690.

A digital thermometer, DTP1000, used with a platinum resistance probe, provides accuracies of better than 0.1 C. Resolution is 0.1° with a total excursion of ±199.9, and 1° for a total excursion of ±1999. The unit works with platinum resistors conforming to BS 1904, DIN 43760 and IPTS 68. The seven-segment display provides open-circuit indication. A built-in bridge conditioning circuit has a stability of 0.01°C/°C. Case dimensions are 48 × 96 × 100 mm, with a DIN panel cutout of 44 × 92 mm.

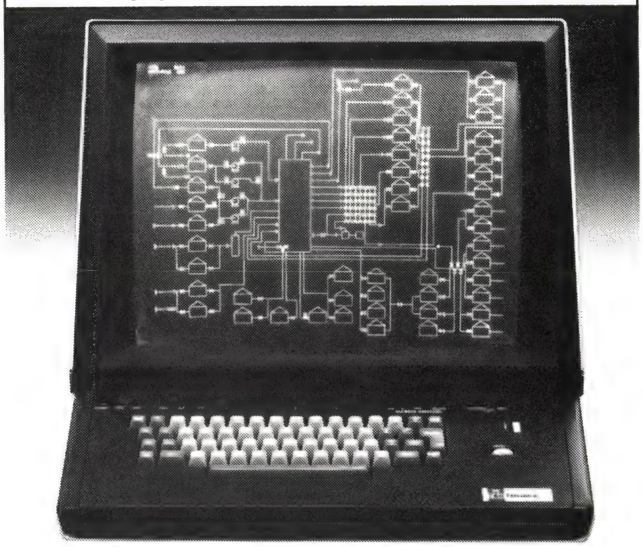
CIRCLE NO. 513

OEMs
"talk to Tektronix"
for a full range of graphics

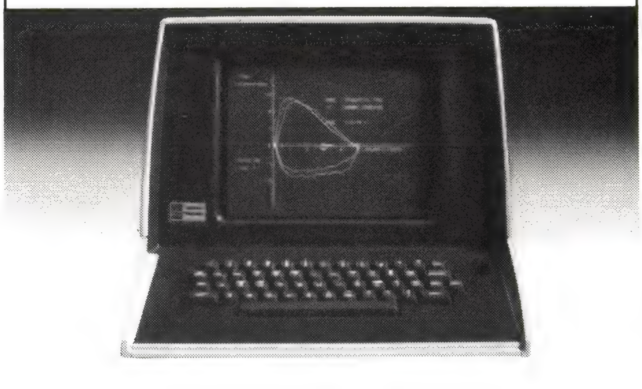
4020 series – enhance applications such as business management through graphics representation & colour.



4014 – high-resolution, large-screen interactive graphics. The most popular with OEMs.

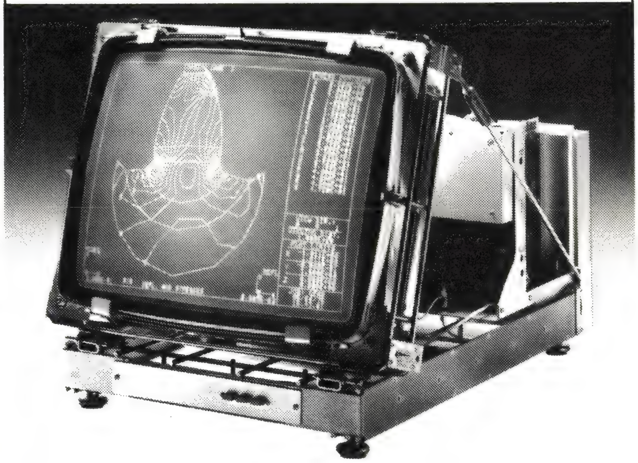


4006 – our lowest cost graphics terminal.



4050 series – powerful computers for data acquisition and analysis.

GMA series – modular displays giving the OEM customer flexibility in system configurations.



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1180 AV Amstelveen, The Netherlands. Tel. 020 471146

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4020 series	☐	GMA series	☐
4014	☐	General graphics	☐

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CIRCLE NUMBER 138

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Eindhoven, The Netherlands

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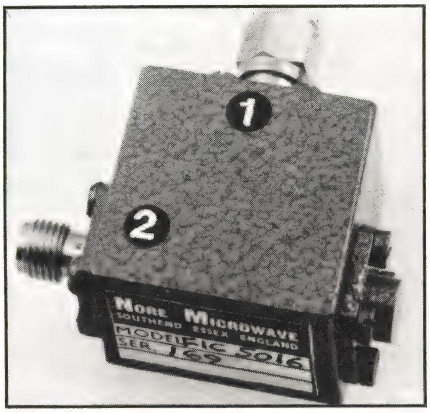
CIRCLE NUMBER 137

International New Products

Tiny microwave isolator covers the L band



Nore Microwave, 36 Towerfield Rd., Shoeburyness, Southend-on-Sea, Essex, SS3 9KT, England. Shoeburyness (03708) 4255

A miniature isolator, measuring only 1 × 1 × 5/8 in., covers a frequency range of 1.2 to 1.7 GHz. The device provides 20-dB isolation and 10% bandwidth. Insertion loss is 0.4 dB. A standing-wave ratio of 1.25 to 1 is maintained over the operating temperature range of −41 to +85 C. Available with a variety of coaxial connector types, including plug-ins, the unit weighs only 1.5 oz. It is completely shielded, and has a load rating of 1 W.

CIRCLE NO. 518

Multipen plotter has its own microprocessor

N. V. Philips Gloeilampenfabrieken, Science & Industry Div., P. O. Box 523, 5600 AM Eindhoven, The Netherlands. Telex: 51573

A multipen digital plotter, PM8151, offers a programmable choice of eight pens, including standard drafting pens and various-color felt-tip pens. Designed to produce quality technical drawings, the plotter is controlled by a Zilog Z80 microprocessor for simple operation and programming. Examples of the capabilities include linear interpolation for vector generation, absolute and relative plotting and circles and arcs—clockwise or counterclockwise. Up to 120 different characters—upper or lower case—can be printed using five different fonts. Plotting area is 280 × 338 mm, with a full-scale accuracy of 0.1% and a linearity of better than 0.1%. Grid marking and X-Y axis scaling are included in the capabilities. Either V.24 serial or IEEE-488 bus interfacing is available. An 800-byte buffer—extendable by 1 kbyte—provides storage for incoming data. A ROM expansion allows addition of special characters and user-defined subroutines to the standard software. The unit operates on 110, 220 and 240 V ac at 50 or 60 Hz, with a power consumption around 30 VA. Dimensions are 160 × 466 × 452 mm, and weight is 13 kg.

CIRCLE NO. 519

Micro-controlled machine programs all devices

Digitronics Israel Ltd., 3 Tevuot Haaretz St., P.O. Box 39821 Tel-Aviv, Israel. (03) 472010. Telex: 35770.

Controlled by an internal microprocessor, the UP-803 universal programmer will read, program and verify all programmable devices. The devices are grouped into a few large families; each family is handled by a single FAM family module. Each FAM module can handle several algorithms, which are software selected by a personality switch. Configuration and pinout are selected by a low-cost DA device adaptor. The machine operates interactively through a hexadecimal keyboard and a CRT display. It handles devices with over 24 address and 16 data lines, and with capacities exceeding 288 kbits. The UP-803 interfaces with all popular address and data formats, including those of all development systems. Suitable FAM and DA units will be made available for new programmable devices as they are introduced.

CIRCLE NO. 520

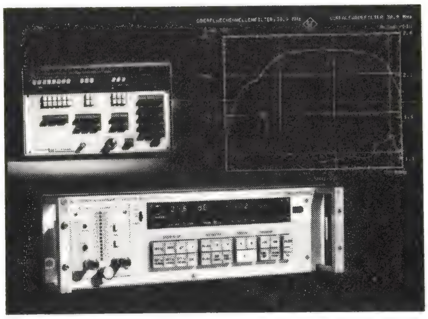
Bubble-memory board packs a megabit of data

Intel Corporation (UK) Ltd., 4 Between Towns Rd., Cowley, Oxford OX4 3NB, England. Oxford (0865) 771431. Telex: 837203.

The IMB-100 bubble-memory board stores 1 Mbit and works with Intellec Series II development systems or any system that uses the Intel Multibus. The board employs the 7110 bubble device. An 8085A microprocessor on the bubble-memory board acts as a memory controller. The CPU in the development system communicates with this controller via a set of registers using normal I/O commands. The 8085A controls system timing and various analog circuits that access the bubble memory. A series of test programs on a double-density floppy disk are supplied for exercising the memory. The IMB-100 can be operated at temperatures from 0 to 50 C and requires power supplies of ±12 and +5 V dc.

CIRCLE NO. 521

Measuring system aids network analysis to 1 GHz

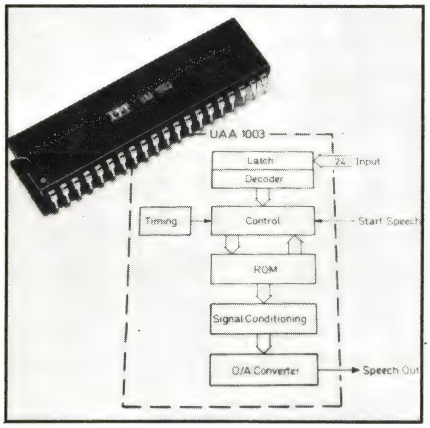


Rohde & Schwarz GmbH, Mühldorfstr. 15, D-8000 Munich 80, West Germany. (089) 412926.25, Telex: 523703

A new kind of network-analysis system, for frequencies up to 1 GHz, consists of the ZPV vector analyzer, the SMS signal generator and a conventional calculator. Features of the automated system include faster measuring rates, compared to similar equipment, simple generation of measuring programs, low price, and improved measurement accuracy through calculator correction. Operating frequencies can be optionally extended to 2 GHz. Impedance can be measured by an entirely new means—the Tee method—without the use of bridges or directional couplers. Results can be read out directly in the required units. This type of complex measurement can be made in less than 40 ms. Available S-parameter correction software minimizes the effects of errors in various instruments. The ZPV's built-in d/a converter provides an output for a recorder; the calculator is not needed for a printout.

CIRCLE NO. 522

Synthesize human speech with a single VLSI chip

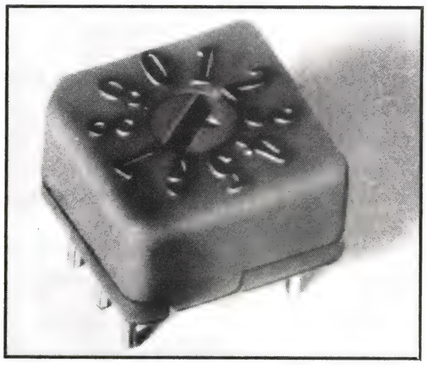


ITT Semiconductors, Maidstone Rd., Footscray, Sidcup, Kent DA14 5HT, England. (1) 3003333. Telex: 21836

A VLSI chip, UAA 1003, generates human speech for consumer applications such as talking clocks, telephone responders and audible warnings for automobiles. Storage and processing of the speech is completely digitized. Several complex methods of data reduction make it possible to include all the necessary speech elements for a vocabulary of about 25 words, plus the control circuitry, on a single chip. Various languages and vocabularies can be accommodated by mask programming of the basic chip. The first version will be used in a talking clock application.

CIRCLE NO. 523

Tiny BCD switches mount on PC boards

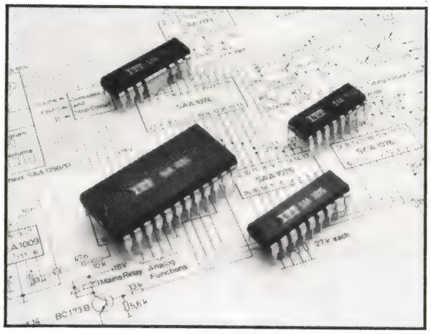


DAU (UK) Ltd., Church House, 94 Felpham Rd., Felpham, Bognor Regis, West Sussex PO22 7PG, England. Bognor Regis (02433) 25141. Telex: 86843

Series-422, BCD-coded subminiature switches, are designed for mounting on PC boards. The 422-10 is a dual-in-line type, approximately 10-mm square with a maximum height of 8 mm. An in-line, horizontally adjustable version is slightly larger with dimensions of 11.6 × 10.2 × 7.7 mm. The switches are sealed to prevent contamination during manufacture or when soldering. The body and base plates are welded together. A reliable contact system uses hard, gold-plated bronze balls working between the contact springs. Mechanical life is in excess of 10,000 operations. In addition to BCD and complementary BCD, hexadecimal coding is available.

CIRCLE NO. 524

IC kit provides parts for digital tuning of TV



Intermetall GmbH, P.O. Box 840, D-7800 Freiburg, Federal Republic of Germany. (761) 5171. Telex: 772715.

A kit of ICs provides all the major parts needed to assemble a phase-locked-loop (PLL) TV frequency synthesizer for digital tuning, program storage, station searching and display of channel number on the screen. The kit consists of the following parts: SAA 1074, control IC; SAA 1075, MNOS memory; SAA 1076, MOS display; SAA 11733, programmable uhf divider and amplifier. The synthesizer kit can be used in conjunction with a remote-control kit to design advanced TV receivers for new applications, such as teletext, viewdata and video games.

CIRCLE NO. 525

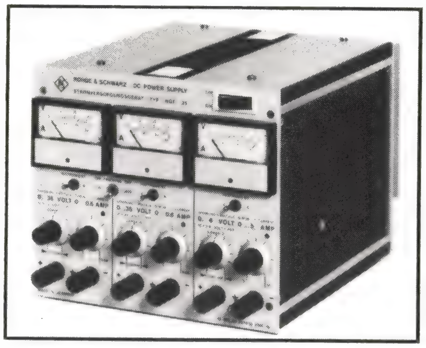
Bus-compatible controller gives µCs disk memory

Intel Corp. (UK) Ltd., 4 Between Towns Rd., Cowley, Oxford OX4 3NB, England. Oxford (0865) 77143. Telex: 837203.

A disk controller, iSBC 206, provides an interface between the Intel-SBC range of single-board microcomputers and hard-disk drives of the IBM-5440 type. The iSBC206 interfaces directly with the Multibus and comes as two boards: a channel board and an interface board. The channel board, the interface to the Multibus, contains its own microprocessor, command decode circuitry and DMA control. The interface board, the interface to the disk drive, serializes and deserializes parallel data for read/write operations as well as carrying out CRC error-detection calculations. The iSBC206 will control up to four 5440-type drives—giving a total memory capacity of 40 million bytes per controller. It operates with either 16 or 20-bit addresses and with either 8 or 16-bit data-bus widths. Each of the two boards is 12 × 6.75 × 0.5 in. (30.48 × 17.15 × 1.27 cm), and weighs 1.75 lb (0.8 kg). Power required is 5 V dc ±5% with a typical current of 5.5 A.

CIRCLE NO. 526

Triple-output power supply delivers up to 35 V



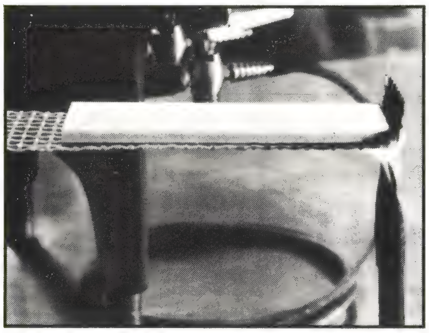
Rohde & Schwarz GmbH, Mühldorfstrasse 15, Postfach 801469, D-8000 München 80, Federal Republic of Germany. (089) 41292625. Telex: 523703

A triple-output supply, NGT 35, costs the same as an earlier model, NGT 20, yet has two outputs adjustable from 0 to 35 V instead of 0 to 20 V. As with the earlier supply, the third output is 6 V. Output power ratings are identical for the two supplies. The supply is primarily intended to supply digital and linear ICs simultaneously. Also, the ±35-V outputs make the unit suitable for analog power circuits requiring voltages higher than the usual ±15 V of linear ICs. All outputs have independent switchable meters and

LED indication of current limiting. The 35-V outputs can be used separately—in series or parallel—as well as in a tracking mode. The 6-V output features overvoltage protection with an adjustable threshold.

CIRCLE NO. 527

Polyurethane resin forms fire-retardant material



Emerson & Cuming (U.K.) Ltd., Colville Rd., Acton, London WC, England. (01) 992-6692.

A polyurethane foam-in-place resin, Eccofoam FPH-FR, cures to a rigid fire-retardant material that has high strength at elevated temperatures. The material is useful for electronic encapsulation, void filling and a variety of structural applications where high-temperature properties are important. Once cured, it will withstand continuous exposure to 275 F (135 C). For short periods it will withstand 325 F (163 C). The material has excellent adhesion to a wide variety of materials—a useful property when it must remain in the cavity that it fills. The foaming reaction is started by mixing the liquid resin component with a catalyst. Foaming begins within a minute.

CIRCLE NO. 528

ECL prescaler circuit accepts inputs to 125 MHz

N.V. Philips Gloeilampenfabrieken, Elcoma Div., P.O. Box 523, 5600 AM Eindhoven, The Netherlands Telex: 51573

An ECL programmable-ratio prescaler, SAA1058, which divides by 32 or 33, is intended for use in digital radio tuning system and frequency-counter instruments. It has a total input frequency range from 0.5 to 125 MHz, and handles AM or FM signals. The chip includes a differential wideband preamplifier which allows it to work with AM input signals from 5 to 100 mV (0.5 to 30 MHz) and FM signals from 10 to 100 mV (30 to 125 MHz). The SAA1058 divides by 32 or 33, depending on whether the control voltage is less than 2 V or greater than 3 V, respectively. Housed in a 16-pin DIP package, the circuit works with supply voltage from 4.5 to 5.5 V.

CIRCLE NO. 529

Five-blade fan withstands voltage fluctuations

ETRI Fans, 3 Guildford Rd., Horsham, Sussex RH12 3JT, England. Horsham (0403) 68797/8 Telex: 877235.

A five-blade fan, 148VK02, maintains high efficiency, even when the supply voltage drops to 208 V from a nominal 240 V. The unit measures 172 × 150 × 38 mm and incorporates an integral capacitor. Nominal speed is 2800 rev/min at 240 V, 50 Hz. At this speed, maximum delivery is 100 litres/s with a maximum static pressure of 18 mm of water. For 60-Hz operation, the corresponding specifications are 3200 rev/min, 117 litres/s and 21 mm of water. The impellor blades of self-extinguishing, glass-filled, thermoplastic meet UL standard UL94VO for flammability. Mounting is by two flanges and electrical connection is by solder terminals.

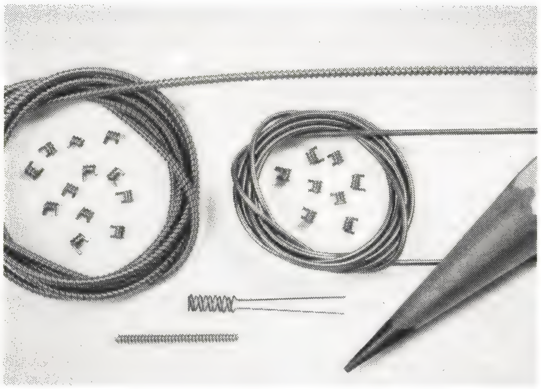
CIRCLE NO. 530

Surge-protection devices now come in smaller size

Cerberus AG, CH-8708, Männedorf, Switzerland.

A new series of gas-discharge surge protectors, type UB, has a tiny metal-ceramic package measuring only 8 × 6 mm. The devices, however, offer the same ratings as the older UC series (8 × 8 mm). Protectors are available with spark-over voltages from 90 to 1500 V, and in both plug-in and wire-ended versions. The devices feature high discharge capacity and fast response.

CIRCLE NO. 531



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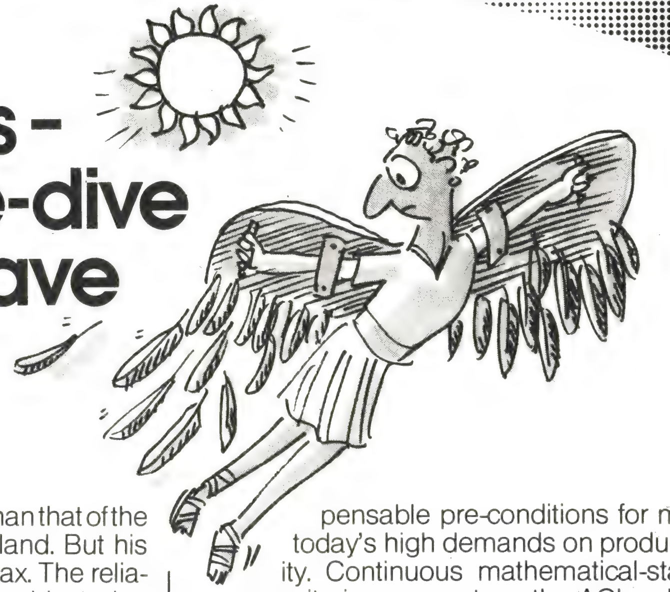
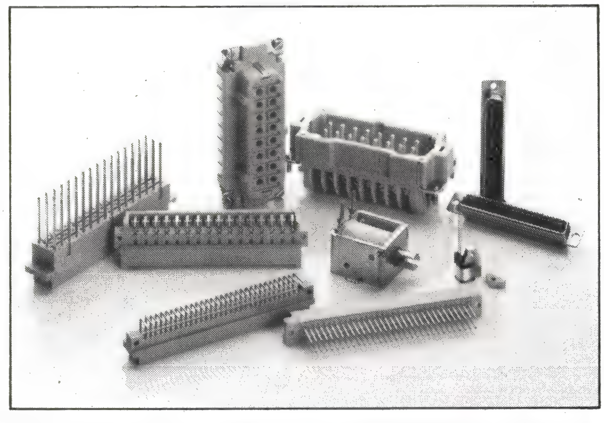
CIRCLE NUMBER 140

Icarus - Or: the nose-dive we could have prevented.



His basic concept was no worse than that of the Wright brothers, Dornier or de Havilland. But his downfall was a component – beeswax. The reliability of this component failed when subjected to extreme operational conditions.

And the absolute reliability of even the smallest, seemingly most insignificant components is an essential today too in the age of large-scale series production.



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WACHTER BREMEN

CIRCLE NUMBER 139

Multiplexed LCD imaging panel delivers 1.5 × 1.5-in. controllable display area

Dave Bursky
Semiconductors Editor

Cockroft International, 777 N. Pastoria Ave., Sunnyvale, CA 94086. Ellafe Kiamco-Cockroft (408) 739-5720. P&A: See text.

The CII-101-M multiplexed LCD panel from Cockroft provides a 1.5 × 1.5-in. display area offering 1024 individually controllable display points. Built from twisted-nematic field-effect materials, the display can operate at ac drive frequencies of approximately 1 kHz—about four times the frequency possible with other liquid-crystal technologies. As a result, data fed to the control circuits can be transferred at 32 kHz.

Organized as a 32 × 32 X-Y matrix, the display panel requires just 64 interconnects—32 for the rows and 32 for the columns. The display is reflective, with a visual appearance of black points on a clear (or transmissive) background. Each "point" is actually a 40 × 40-mil spot, with 5 mils separating each point, both vertically and horizontally.

Since the panel requires ac drive, and appears as a capacitor even when no points are visible, the display requires less than 1 μA of quiescent current and drains just 4 μA of active current with half the points visible. The main supply voltage (V_{DD}) ranges from 6 to 7 V. For the row drive, the voltage requirements are a square wave ranging from 0.32 to 0.68 of V_{DD} that is symmetrical around 0.5 V_{DD}. The column drive, on the other hand, requires a square wave that goes from 0 to V_{DD}, but is also symmetrical around 0.5 V_{DD}.

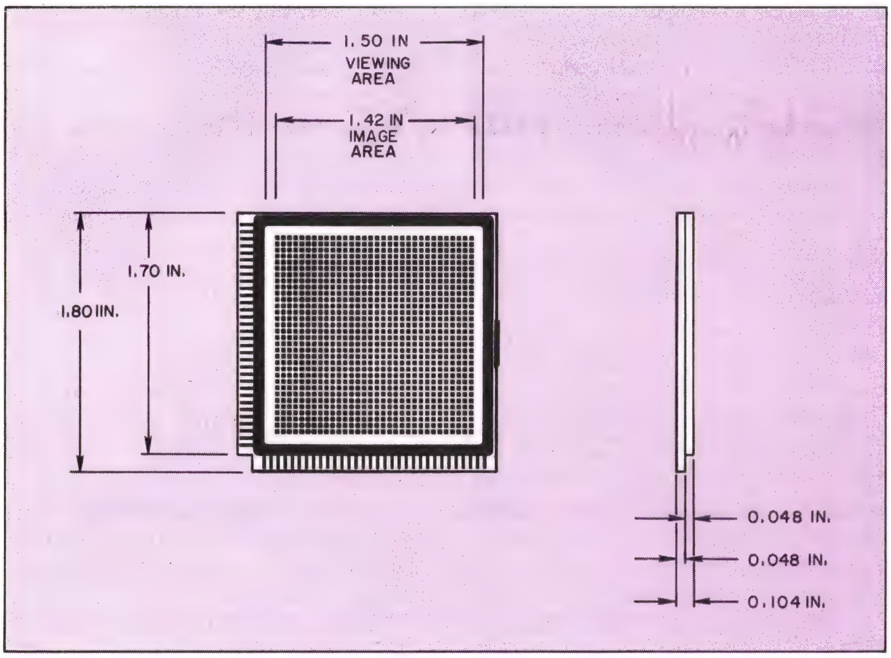
The LCD array can operate over −5 to +60 C—a major improvement over polarized displays, which are limited to 0 to 45 C. In addition, watch for LCD-technology improvements to permit temperature compensation in the materials—the result will be a 15-C extension of the operating range in both directions.

The drive electronics for the array is relatively simple. Row-drive requirements are satisfied by the HLCD-0438 CMOS LSI circuit by Hughes Aircraft (Irvine, CA). This circuit contains a 32-bit shift register (serial-in, parallel-out), output latches and Exclusive-OR gates. However, for the column drive, the control ciruits have to be pieced together from CMOS MSI (four 8-bit serial-in, parallel-out shift registers, 11 triple two-channel analog multiplexers, and about a half dozen other CMOS ICs).

The electrode structure in the array is designed so that each drive line is shared by the 32 elements in the X direction, and similarly in the Y direction by the corresponding drive line. For a point to be turned on, both the X and Y voltages must be at their maximum levels so that the voltages, when combined, exceed the LCD-material threshold. Incidentally, other array organizations besides 32 × 32 are simple to develop.

With the current unit, display colors can be changed by adding a polarizing filter, either during manufacture or end-product assembly. Eventually, however, variable colors will be available simply by combining a precisely controlled drive with voltage-sensitive pleochroic dyes, slated for introduction later this year.

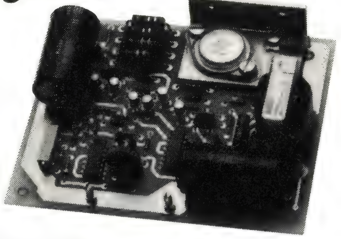
Initial samples of the 32 × 32 CII-101-M will not come cheap—the display with mating connectors, minimum electrical interface card and detailed application notes costs about \$150. However, projected high-volume costs for the 32 × 32 array should see prices drop to below \$3.00 per unit in million-piece orders. In the works, meanwhile, is an interface board containing the display and the basic electronic drive circuits. The bare-bones unit takes two weeks to deliver.



Built with liquid crystals, this imaging array offers a full 1.5 X 1.5-in. display area made up of 1024 individually controllable points. The display panel requires only 64 interconnects.

CIRCLE NO. 301

Boschert's 3T Switching Regulator



3T-12AP-1001

Size:	5″ x 4.1″ x 1.7″ max.
Input Voltage:	10 to 40VDC (60 Hz bulk source or battery)
Output Voltage:	4.5 to 30VDC (adjustable)
Output Current:	0 to 12A
Efficiency:	80% typical
Regulation:	±1% (15 to 40VDC), 2% (10 to 40VDC)
Current Limit:	5A to 20A (adjustable)
Price:	$30 in quantities of 100 Available from stock

3T-5AN-1001

Size:	5″ x 5.4″ x 1.7″ max.
Input Voltage:	10 to 40VDC (60 Hz bulk source or battery)
Output Voltage:	−4.5 to −30VDC
Output Current:	0 to 5A
Efficiency:	80% typical
Regulation:	±1%
Current Limit:	1A to 10A (adjustable)
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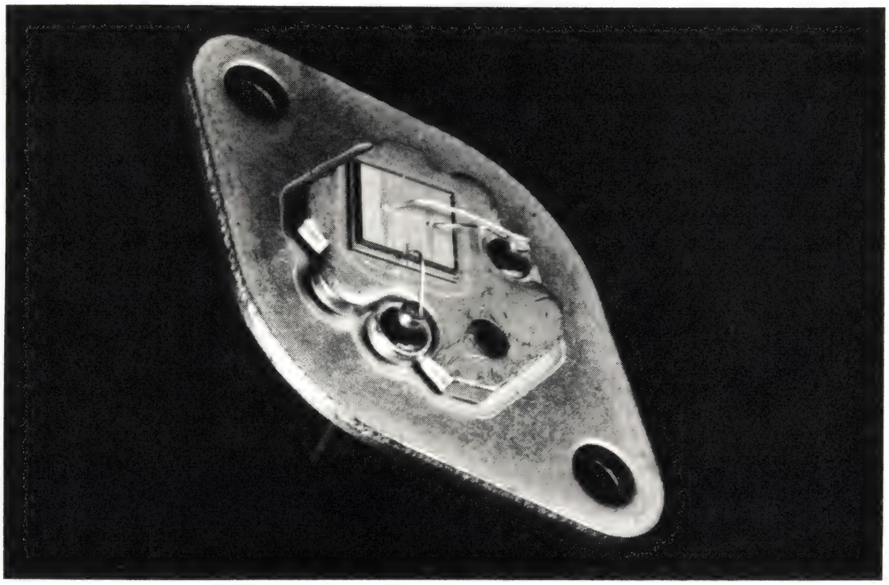
Process breakthrough gives high-breakdown MOSFETs



Supertex, Inc., 1225 Bordeaux Dr., Sunnyvale, CA 94086. Richard Blanchard (408) 744-0100. P&A: See text.

Built with a vertical-MOS, or DMOS, manufacturing process, power MOSFETs from Supertex offer breakdown voltages higher than 500 V. The technique employs field-limiting rings processing methods to distribute voltage across the chip surface. Four transistors in the VN04 family take advantage of the technique to give minimum BV_{DSS} of 500 V (VN0450), 450 V (VN0445), 400 V (VN0440) and 350 V (VN0435).

For high-voltage switching applications, the FET family typically features static on-resistances ($R_{DS(ON)}$) in the range of 0.6 to 0.9 Ω. The maximum value for all devices is 1.0 Ω, measured at a drain current of 4 A and a gate-to-source voltage of 5 V. Small-signal on-resistance ($R_{ds(on)}$) is even lower—typically it spans a range of 0.4 to 0.7 Ω—with a maximum of 0.8Ω, measured with 5-A drain current and 10-V gate-source voltage.

High-current devices all, the family members carry 12 A continuous at a drain-to-source voltage of 25 V. Under pulsed conditions, 20 A can be handled. Gate threshold voltage varies from a minimum of 1.0 V to a maximum of 3.0 V, allowing the FETs to interface directly to TTL or MOS-logic drivers. Input capacitance for the series is 2000 pF typically.

Switching-time specifications are the same for each device in the family: Turn-on delay is 40 ns, rise time 90 ns; turn-off delay time is 150 ns, and fall time 100 ns, all typical. Switching-time tests are performed with a drain current of 1 A at a drain-to-source voltage of 25 V.

A range of applications includes switching power supplies as well as power and industrial control equipment that operates directly from the 115-V ac line.

The first VN0400s, available now, will be packaged in TO-3 cans, but dice are available for either hybrid or in-house applications.

Pricing, for a TO-3 packaged 450-V VN0 445, is $31.74 in quantities of 1000. At 50,000 pieces, the price goes down to $24.

CIRCLE NO. 302

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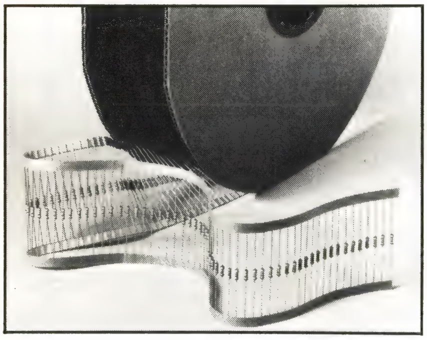
boschert SWITCHING POWER SUPPLIES

CIRCLE NUMBER 59

Metal-film resistors bring improved tolerance, tempco to general use



Mepco/Electra, Inc., P.O. Box 760, Mineral Wells, TX 76067. Peter Robinson (817) 325-7871. P&A: See text.

With the SFR (Standard Film Resistor) 5043E series, Mepco/Electra makes available general-purpose 1/4-W metal-film resistors that boast tighter tolerances and lower tempcos than general-purpose carbon-composition resistors—and at comparable prices.

Metal-film tolerance is ±2%—a far cry from the ±5 or ±10% tolerance offered by similarly priced carbon-comp resistors. The metal-film tempco is easily within ±200 ppm—quite a jump from the ±1000 ppm typically specified for carbon-comps.

What's more, metal-film resistors in general sport greater resistance to changes due to moisture. Moisture resistance, specified according to MIL-STD 202, is typically ±15% for carbon-comps, ±1.5% for metal-films. The SFR-5043E series, however, is tested for "damp heat" resistance change under IEC spec No. 68, so resistance change is even better: less than ±1%.

Available in values of 10 Ω to 1 MΩ, the Mepco/Electra resistors feature a maximum voltage of 250 V. What's more, they are compact—less than 0.260 in. long and 0.098 in. in diameter, with axial leads. In addition, they are available with taped leads for automatic insertion.

The Mepco SFR-5043E resistors cost close to 2 cents each in OEM quantities, compared to 3 or 4 cents for carbon-comps. Delivery is stock to eight weeks ARO.

CIRCLE NO. 303

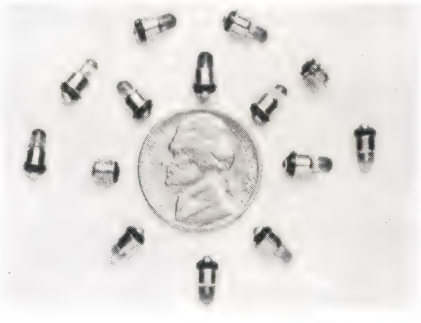
Tuning diode works into microwave region

MSI Electronics, 34-32 57th St., Woodside, NY 11377. (212) 672-6500. $5.60 (100 qty); 3 wks.

A tuning diode, ZC898, offers low capacitance for operation into the low microwave region. At 20-V reverse voltage bias, capacitance is 0.8 pF. At 2-V reverse bias, capacitance is greater than 4 pF for a tuning range of better than 5:1. A Q of 300 at 3 V increases rapidly with reverse voltage to provide low-loss operation at the higher frequencies. The device comes in a DO-7 hermetically-sealed glass case.

CIRCLE NO. 324

LEDs in T-1 packages replace incandescents



Data Display Products, 303 N. Oak St., Inglewood, CA 90302. (213) 674-5940.

Bright LEDs in T-1, submidget flanged packages, MF125, directly replace incandescent lamps of the same package style. The LEDs eliminate burned-out filaments and, because they are rugged, withstand high vibration environments. The devices required an external resistor and exhibit a 2.4-V drop at 20 mA. Red, amber and green versions are available with clear or translucent lenses.

CIRCLE NO. 325

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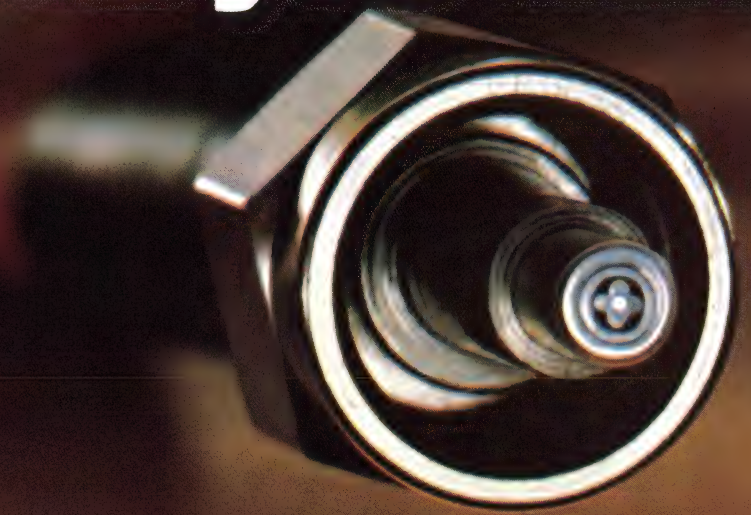

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CIRCLE NUMBER 60

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H-1-8A

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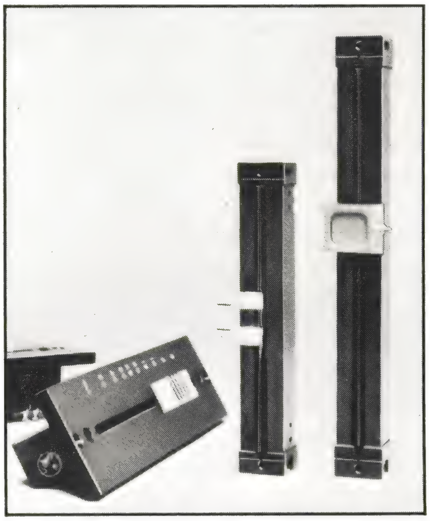
H-1-9

Plastic slide potentiometers stretch resolution, tighten linearity



Duncan Electronics, Div. of Systron-Donner, 2865 Fairview Road, Costa Mesa, CA 92626. Terry Thatford (714) 545-8261. P&A: See text.

A novel formulation of conductive plastic provides infinite resolution, low noise and long-life operation in the 400-series slide pots from Duncan Electronics. What's more, linearity can be as little as ±0.01% with the conductive-plastic resistance element, which is rated to last more than 50-million cycles without exhibiting performance degradation.

The resistance range of the 400-series slide pots is 600 Ω to 250 kΩ. Standard tolerance is ±20%, though ±10% can be ordered, along with ±0.01% linearity. Standard linearity is ±2%.

The outer package is only 5/8 in. wide, making the Duncan 400 slide pots the narrowest available. The pots also come with normally open SPST or DPST switches, which close at the end of travel. And with single or double-wiper elements, two stroke lengths are available: 2-3/4 and 4-1/4 in.

Intended for audio recording and broadcast consoles, the 400-series pots also have the linearity and durability required by test and medical instruments.

Depending on stroke length, wiper configuration and quantity, the pots cost $6 to $12. Delivery is stock to three weeks.

CIRCLE NO. 304

One-gun CRT produces multicolor images

Thomson-CSF Dumont, 750 Bloomfield, NJ 07015. (201) 773-2000.

A single-gun CRT intended for radar display applications, Model TH 8414P49, produces high-resolution, multicolor images. A single electron gun eliminates registration problems. P49 multicolor phosphor permits images in red, orange, yellow and green. The circular-format screen measures 22 in. in diameter.

CIRCLE NO. 326

Switching transistors handle up to 200 W

Panasonic, One Panasonic Way, Secaucus, NJ 07094. Bill Bottari (201) 348-7276. $2.25 (2N5630, 2N6030); $2.85 (2N6250) (1000 qty); stock to 8 wks.

A family of high-current, high-voltage power switching transistors works in such diverse applications as audio output stages and switching power supplies. 2N5630 and 2N6030 are npn and pnp types, respectively, and handle 120 V at 16 A continuous. These types are available in complementary pairs for use in push-pull output stages. Type 6250 operates at up to 275 V and 15 A continuous. The devices come in standard TO-3 metal cases.

CIRCLE NO. 327

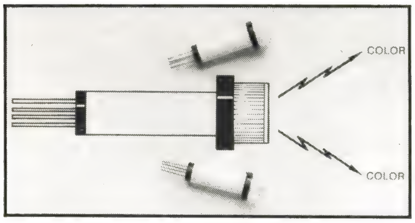
Power attenuator dissipates 50 W in microstrip use

KDI Pyrofilm, 60 S. Jefferson Rd., Whippany, NJ 07981. (201) 887-8100. $25 (100 qty); stock to 6 wks.

First of a series, the PPA 50 flange-mounted attenuator dissipates up to 50 W in microstrip use. The device operates from dc to 1 GHz with a VSWR of 1.2 maximum over the top half of the range. Attenuation accuracy is ±0.3 dB to 500 MHz and ±0.5 dB to 1 GHz.

CIRCLE NO. 328

Front-panel LED uses plastic lens to display two highly visible colors



Data Display Products, 303 N. Oak St., Inglewood, CA 90302. Tony Daniels (213) 674-5940. P&A: See text.

A special, transparent plastic-lens assembly enables a LED assembly to display two colors with no loss in brightness. The Bi-Color panel light from Data Display is available in any combination of red, amber or green for front-panel indications of on-off, stop-go, ONE-ZERO and other two-pole conditions on computers, instruments, industrial process controls and consumer electronics application.

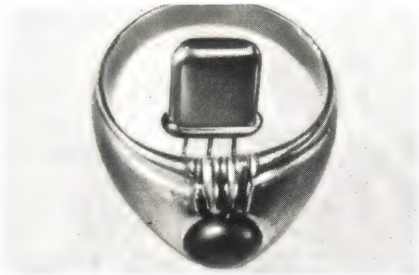
Basically, the 0.920-in. × 0.312-in.-diameter cylinder houses two separate LEDs. Striated lines in the 0.395-in. × 0.39-in.-diameter lens assembly ensure high visibility of either color at a wide variety of viewing angles. Moreover, with two LEDs in one package, there is maximum electrical isolation between LED circuits.

The plastic lens, in addition, protects the LEDs and associated electronics from static discharge damage.

The four-lead package comes in five models, four of which require 3.6 to 28-V power supplies, while a fifth requires 2.4 V and an external load resistor. Models with internal load resistors are priced at $2.90 each in lots of 1000. Delivery is two to five weeks.

CIRCLE NO. 305

Tiny reference crystal fits onto packed boards



Bulova Electronics, 61-20 Woodside Ave., Woodside, NY 11377. (212) 335-6000. $3.09 (1000 qty); stock to 6 wks.

A 1-MHz subminiature crystal, Model 200, occupies only 0.04 in.^{2} on high-density PC boards. The unit is 0.34-in. high with a total envelope volume of 0.0136 in.^{3}. Pin spacing is 0.148 in. Thermal compression bonding of leads to the crystal face eliminate unit-to-unit variations following soldering operation. The crystal enclosure is resistance-welded for hermetic sealing. Tuning tolerance is typically ±25 ppm at 25 C. Standard temperature stability is 100 ppm over a −40 to 70-C range. Tighter tolerances are provided on special order. The crystal cut is DT Bar.

CIRCLE NO. 329

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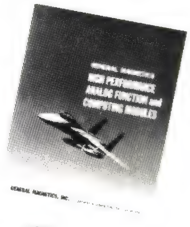
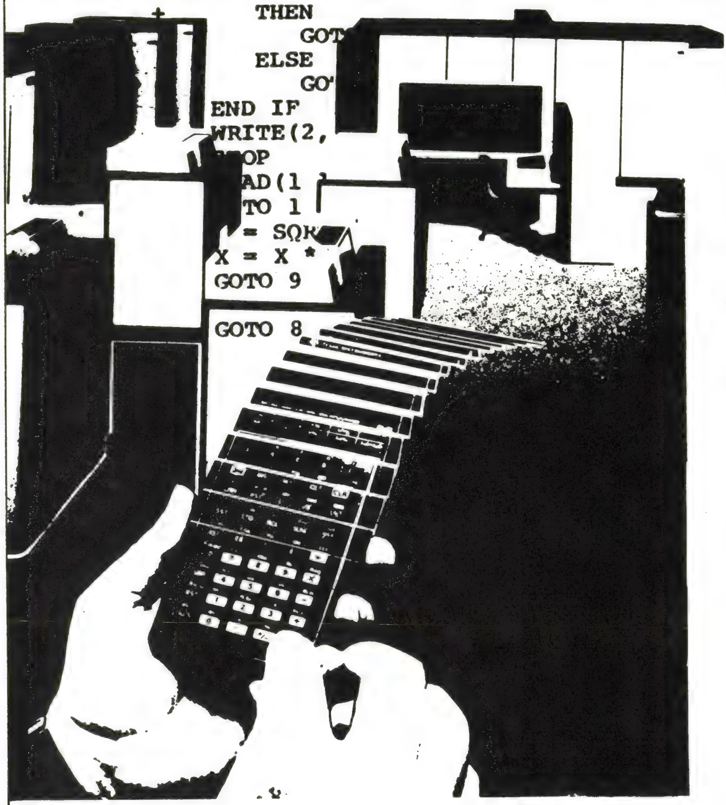


```
      GOTO 3
1     IF (X .EQ. 0.0)
   +        THEN
               GOTO 9
            ELSE
               GOTO 5
         END IF
5        IF (X .GT. MAXVAL)
   +        THEN
```

Hayden simplifies. . .



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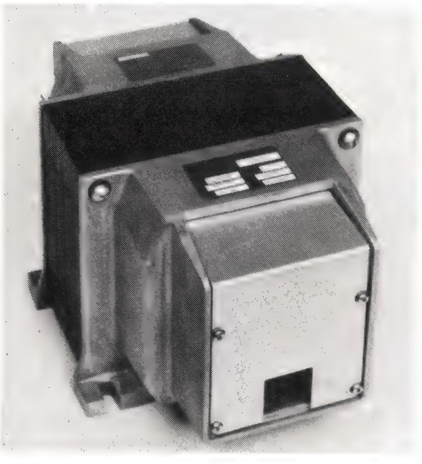
CIRCLE NO. 330

Transformer gives computer-grade power

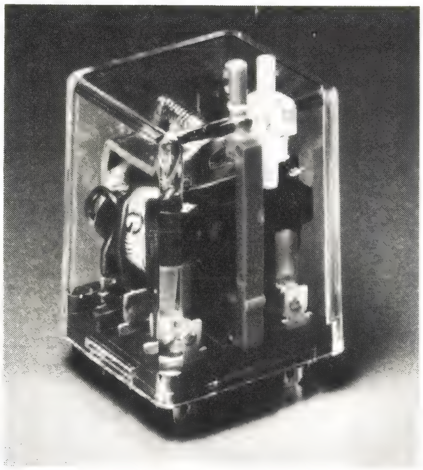


Deltec, 980 Buenos Ave., San Diego, CA 92110. (714) 275-1331.

A series of isolation transformers provides protection and power for computers requiring 250 VA to 5 kVA single-phase and 9 kVA to 15 kVA three-phase. Box shields are placed over both primary and secondary windings. A Faraday shield is placed between them. The primary shield is returned to power ground; the secondary shield, to computer ground; the Faraday shield, to earth or system ground. This increases common-mode rejection to more than 140 dB and intercoupling noise rejection to more than 150 dB. Input-to-output capacitance is less than 0.001 pF. Leakage resistance exceeds 10,000 MΩ.

CIRCLE NO. 331

Test relay load circuits without applying power



Eagle Signal Industrial Controls, 736 Federal St., Davenport, IA 52803. (319) 326-8147. $8.85 to $31.25.

A push-to-test button on a series of control and time delay relays permits load circuit testing without use of the relay's drive circuit. A manual reset button provides latch/reset control functions without additional circuit components. The two-button combination is offered on Series 30 general purpose relays in 5-A, 10-A and low-level models. The feature is found on Series 31 dc current-sensitive versions and on Series 39 time delay units with the same contact ratings. Polyurethane magnet-wire insulation enhances heat dissipation. The relays are dust and moisture-resistant and offer 500-V rms (60 Hz) dielectric strength between open contacts. Typical pull-in speed is 12 ms; drop-out speed, 10 ms. The units are rated for continuous duty cycle.

CIRCLE NO. 332

Modular design extends piezo alarm choices

Floyd Bell Associates, P.O. Box 12327, Columbus, OH 43212. (614) 488-3193.

A modular approach to piezo-electric sound devices permits a choice of many right-for-the-job 2300 Series alarms. Seven circuits, three alarm modes, four mounting styles, three body depths, three terminal systems, three voltages and four different front caps create hundreds of different alarms. The devices are tamper-proof and operate under adverse conditions, including extremes of cold or humidity. Optional alarm modes include continuous tones, beeps and warbles. An acoustic volume control option permits simple adjustment of an alarm's output.

CIRCLE NO. 333

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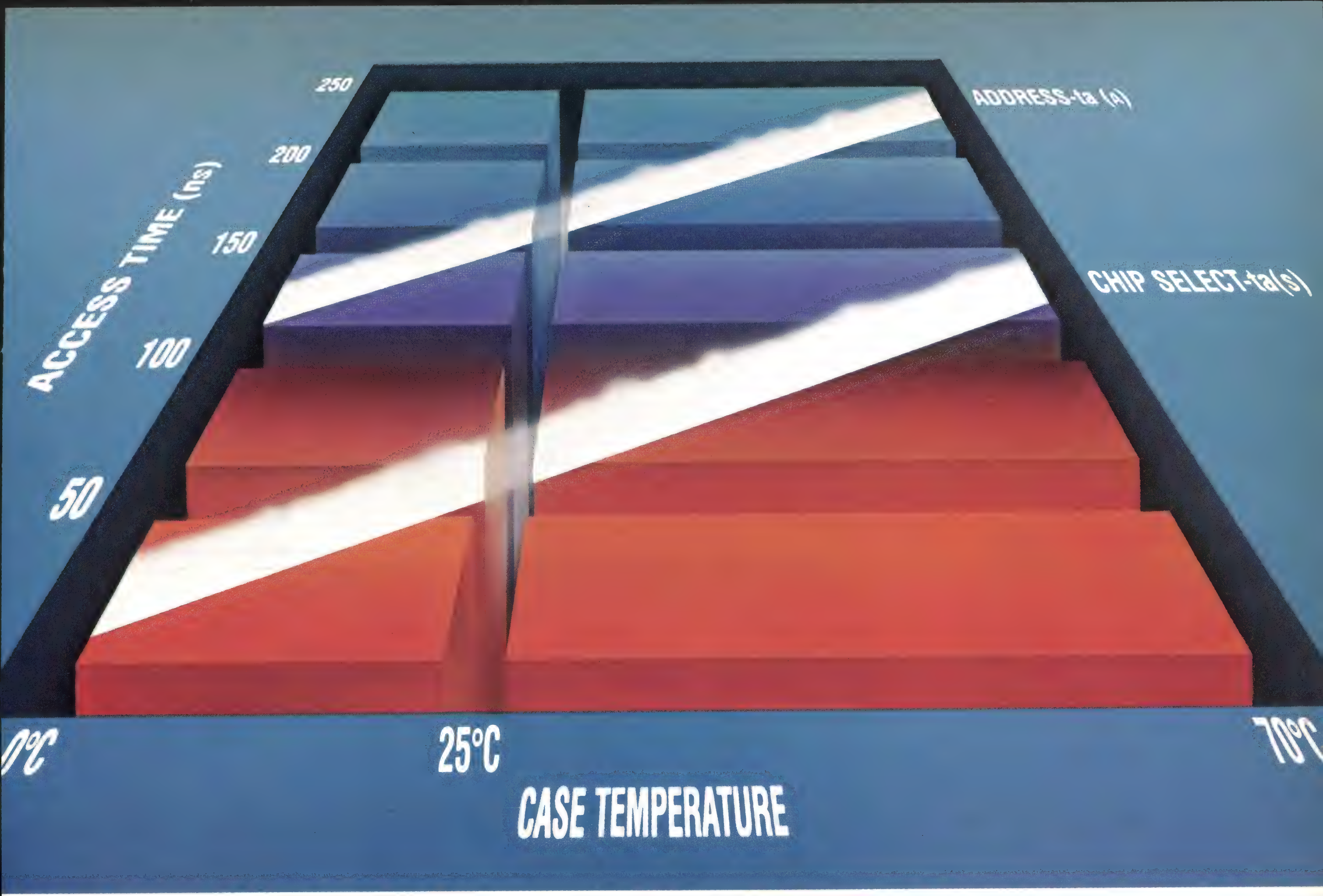

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At 250-ns max access time, 180-ns typical, the TMS2508 is the fastest EPROM on the market. So fast, in fact, that you can design it in for all state-of-the-art microprocessors and not worry about sacrificing performance. The TMS2508 reduces wait states and virtually eliminates the need for any additional wait-state circuitry.

As a bipolar alternative

Because the TMS2508 is so fast, it also allows you to implement many memory applications previously served only by bipolar PROMs. Only minor board modifications are required to make the switch from bipolar to MOS. (For complete details see Applications Note MM-2508.) And, unlike PROMs, the TMS2508 can be easily and quickly erased and reprogrammed. At any time.

High performance

In addition, the TMS2508 offers you such outstanding performance features as 8-bit word configuration, automatic chip select/power down and fully static operation.

So, if speed is what you need, go ahead and design with confidence. Go ahead and specify TI's new TMS2508.

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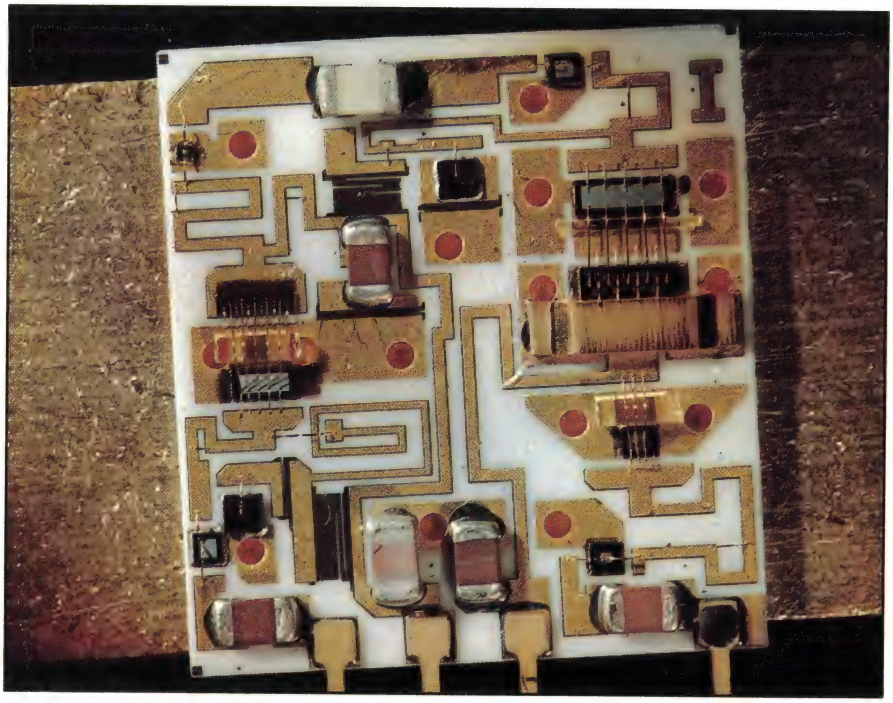

Motorola Semiconductors, Inc., P.O. Box 20912, Phoenix, AZ 85036. Alan Wagstaffe (602) 244-6394. P&A: See text; stock.

Two new Motorola hybrid power amplifiers designed for mobile cellular-radio communications, the MHW-820 and MHW-808, provide 20 W and 7.5 W of wideband power between 800 and 900 MHz. What's more, both modules not only feature the stability and ruggedness required of mobile radio parts but cut the design time, inventory, documentation and assembly costs that would have been required by discrete parts.

Either module can be used as an output stage or as an output-stage driver. Input and output impedances are already matched to 50-Ω sytems, yet a load mismatch, even for a 30:1 VSWR, does not degrade power output —regardless of signal phasing.

The MHW-820 contains three cascaded amplifier stages, set in a common-emitter configuration, that provide at least 19 dB of gain and 20 W of wideband rf power. At full power output, input power is 250 mW max, and harmonic distortion is 58 dB down or better. Stability is 250 mW input or less, with a load VSWR up to 4:1. In addition, spurious signals are held to −70 dB or better. In a 50-Ω system, the MHW-820 amplifier's input impedance will not create a VSWR greater than 2:1, and its quiescent current drain is 125 mA or less.

Similar in specs to the 820, the MHW-808 has two cascaded stages, a minimum gain of 14.8 dB, and maximum harmonics of −52 dB.

Since they are both designed especially for mobile, cellular-radio installations, the amplifiers are rated for operation between −30 and +100-C case temp and from power supplies of 12 to 16 V dc. All operation parameters are specified over the FCC-defined cell-trunk bandwidth of 806 to 870 MHz.

Inside the amplifiers, Motorola has put transistors similar to those in the company's standard product line, albeit processed with different starting materials and diffusion schedules. They are gold-metalized and silicon-nitride-passivated. For enhanced reliability, they are operated at current densities less than 1.5×10^5 A/cm^2.

In 100-quantities, the MHW-820 costs $58, the MHW-808 $41.

CIRCLE NO. 306

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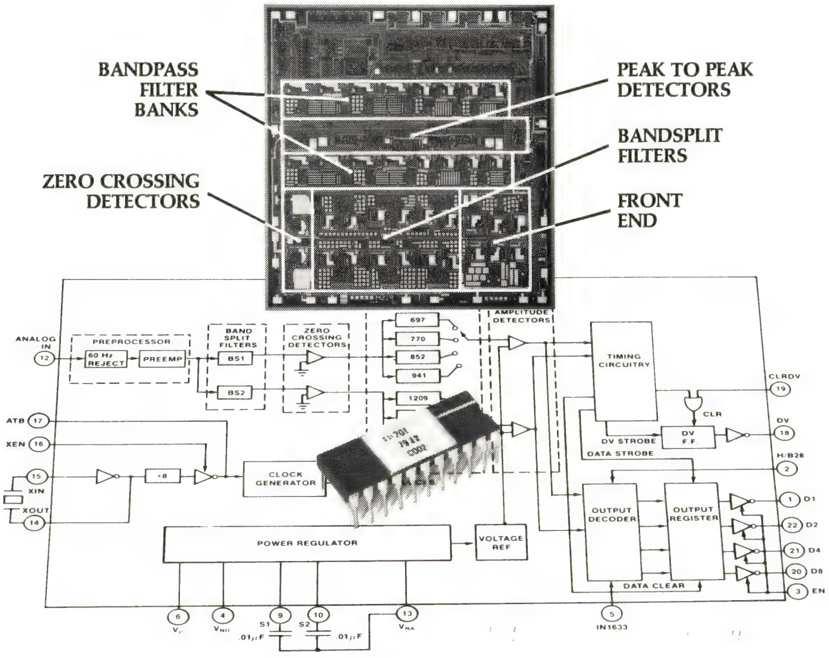

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*(Described in the paper "A Monolithic Dual-Tone Multifrequency Receiver—WAM2.6" presented at the February 1979 International Solid State Circuits Conference.)

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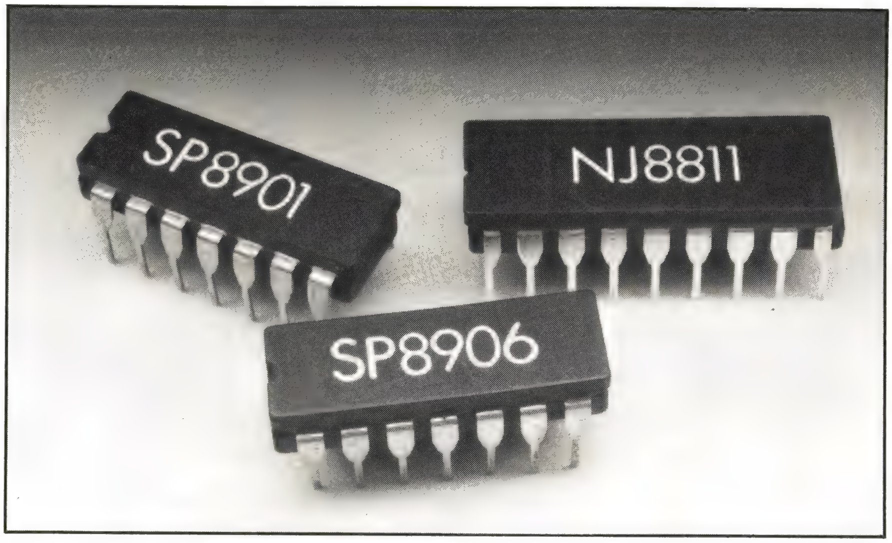
CIRCLE NUMBER 65

Synthesizer chip set permits any radio-channel spacings



Plessey Semiconductors, 1641 Kaiser Ave., Irvine, CA 92714. Bob Greenwood (714) 540-9979. P&A: See text.

With just three ICs, designers can now synthesize all channel spacings needed for radio communications. Aimed at mobile radios, scanning receivers and μP-controlled synthesizers, the chip set consists of the SP8901 four-modulus divider (divide by 512, 510, 480, 478) or the SP8906, also a four-modulus divider (divide by 256, 255, 240, 239), and the NJ8811 synthesizer-controller/divider.

A complete tuner/synthesizer can be constructed simply by selecting one of the dividers and mating it to the NJ8811 and its crystal oscillator (up to 4.8 MHz). A reference divider on the NJ8811, when preset to any one of 16 ratios, will, with a 4.8-MHz crystal, provide channel spacings of 40, 50 and 60 kHz as well as submultiples down to 5, 6.5 and 7.5 kHz.

The 8901 and 8906 can be programmed logically to divide by any one of their four ratios, with the 8901 accepting inputs up to 1 GHz and the 8906 limited to 500 MHz. The NJ8811, which contains all the decoding and control, can be interfaced directly to ROMs, PROMs and microprocessors.

Both the SP8901 and 8906 are housed in 14-pin DIPs and have self-biasing clock inputs. The divider consists of an input amplifier, two cascaded divide-by-15/16 counters and an output circuit. Operating from 5-V supplies, the 8901 requires about 500 mW, the 8906 a slightly lower 400 mW. The output drivers can sink 3 mA or source 5 mA, and have separate power-supply connections to minimize input/output coupling problems.

The NJ8811 comes in an 18-pin DIP and draws just 60 mW. It includes two on-chip 4-bit dividers that can control the modulus of external prescalers, while another 8-bit divider determines the count period.

When the SP8906 is used in conjunction with the NJ8811, the combination can divide an input frequency by all integers between 3480 and 69,375. Grounding one of the control pins on the NJ8811 can offset the range to span all integers from 36,608 to 102,143.

All three circuits operate over −30 to +70 C and are available in sample quantities. In 100-unit lots, the costs are \$10.35 for the NJ8811, \$38.40 for the SP8901, and \$19.20 for the SP8906. Sample deliveries are from stock.

CIRCLE NO. 307

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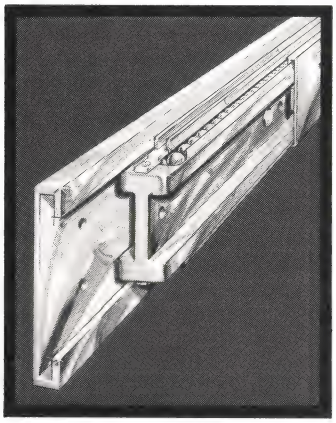
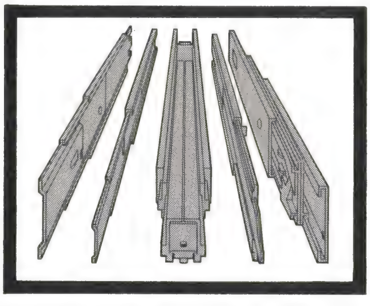
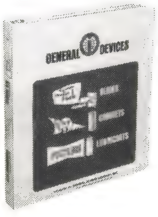

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CIRCLE NUMBER 68

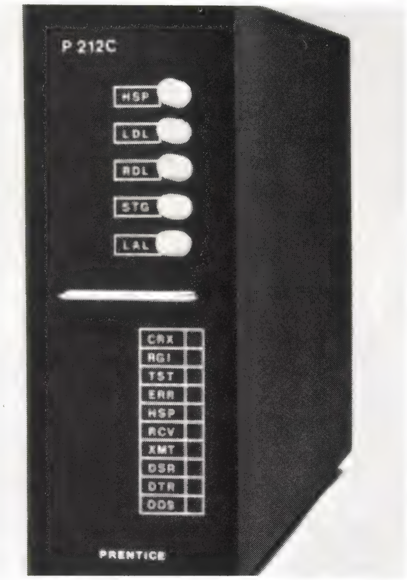
Modem answers short-haul data-comm needs

Micom Systems, 9551 Irondale Ave., Chatsworth, CA 91311. (213) 882-6890. $200; 7 wks.

Asynchronous "dumb" terminals can take advantage of the high-speed transmission capabilities of the Model 410/401 modem. The unit, providing Bell 43401 compatibility, works at speeds to 19,200 bits/s on private metallic circuits. Transmission range is 3 miles at 9600 bits/s and 15 miles at 1200 bits/s.

CIRCLE NO. 334

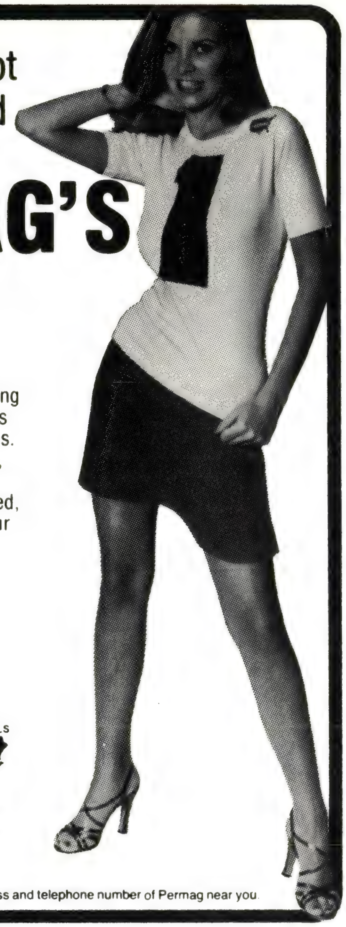
Auto speed select adjusts modems to incoming rates



Prentice, 795 San Antonio Rd., Palo Alto, CA 94303. (415) 494-7225. $895 (P-212A); $1135 (P-212C); 8 wks.

Two dual-speed, dial-up data modems, P-212A and P-212C, automatically adjust operation to match an incoming data rate. Only a 502 or 503-type exclusion key telephone set is required. Both models provide full-duplex transmission of 300 or 1200 bit/s serial binary data over two-wire dial-up lines. Features of the microprocessor-controlled P-212C version include a self-test routine during idle periods. If the modem fails any portion of the self-test, it automatically busies itself out. Also included is a remotely-located failure indicator and manual speed selection. Both modems are available in stand-alone or rack-mount versions.

CIRCLE NO. 335



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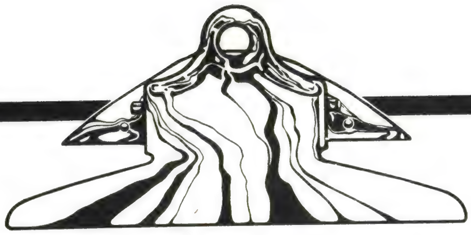

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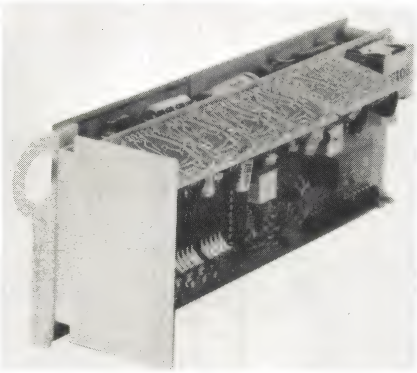
Codex, 20 Cabot Blvd., Mansfield, MA 02048. (617) 364-2000. $13,500.

A voice digitizer, dubbed the Digiphone, converts an audio signal into a 2400 bit/s digital signal. Once converted, the signal can be multiplexed with data and other digital voice signals for reduced communications costs. A dial option digitizes conventional dial and tone signalling to establish standard telephone access to a user's network. Digi-phone is offered for sale or lease.

CIRCLE NO. 336

DTMF decoders plug-in for control jobs

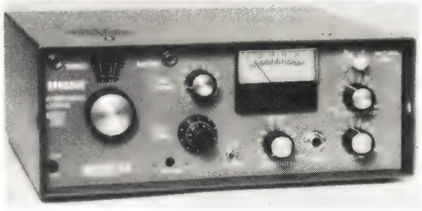


Dantel, 1922 N. Helm Ave., Fresno, CA 93727. (209) 252-1651.

DTMF decoders, intended for order wire and small telephone systems, operate on-board relays for ringing, signalling or other control functions. Models 90709 and 90710 decode two or three digit codes. Model 90710 has an "all-call" function. The PC modules fit 90000 series equipment shelves. Units include an input transformer, three code pre-set switches, a time-out circuit, two dual C-form relays and a strapable pulsing circuit.

CIRCLE NO. 337

Portable receiver spots interference sources



Sprague Micro Tech, 703 Plantation St., Worcester, MA 01605. (617) 852-3515.

A portable interference locator, Model 700, pinpoints interference sources in the 500 kHz to 250-MHz range. Built-in features include a signal meter with sensitivity control, a speaker, a headphone output jack, an external meter output jack and a video display jack for signal tracking with an oscilloscope. Model 700 weighs 11 lb and operates continuously for up to 8 h from a lead-acid battery pack. Accessories include a variety of portable antennas, a hand-held antenna tuner, a high-sensitivity rf probe and a carrying case. Sensitivity is 1 μV or better at frequencies from 2 to 250 MHz and 2 μV or better for all frequencies below 2 MHz.

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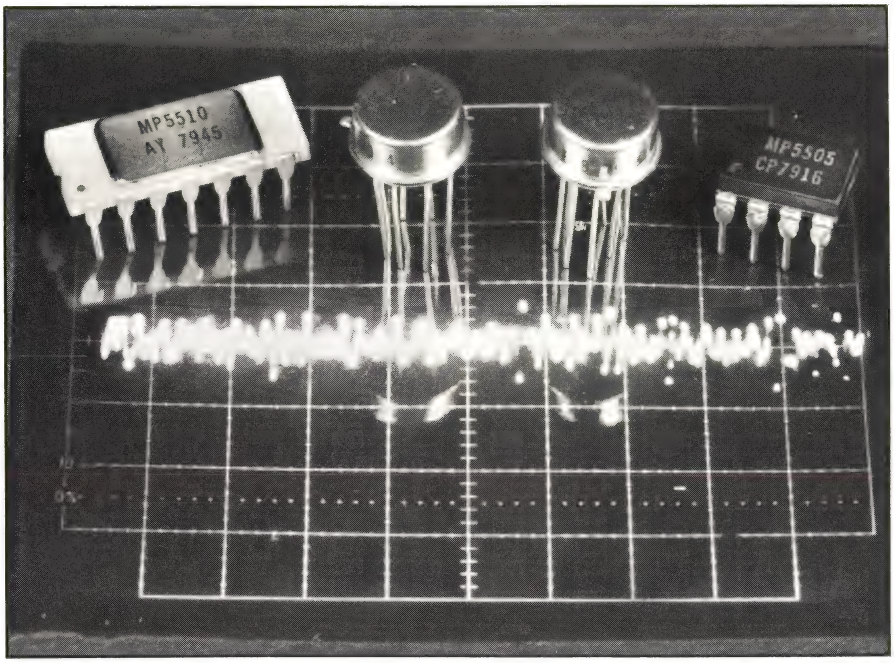
CIRCLE NUMBER 69

Op-amp family jumps ahead —down in noise, up in speed



Micro Power Systems, Inc., 3100 Alfred St., Santa Clara, CA 95050. Mike O'Neal (408) 247-5350. P&A: See text.

Four op amps from Micro Power Systems—three for instrumentation and one a high-speed inverter—boast improved noise and speed characteristics. The MP5505, 5507 and 5510 precision instrument amps yield ultralow input noise and virtually undetectable popcorn noise. The high-speed MP5501 offers a slew rate 50% faster than previous versions of the device.

At 0.1 to 10 Hz, the input noise of the 5505 and 5507 is typically 0.25 μV pk-pk—almost twice as good as that of the OP-05 and OP-07, for which they are pin-for-pin replacements. Input offset voltage (V_{OS}) for the 5505A is only 100 μV, typical, but the 5507E offers an even better specification at 45 μV typical. And when tight offset voltage matching is required, the 5510A, a dual op amp, packs two high-performance amplifiers under one roof with a ΔV_{OS} of 70 μV.

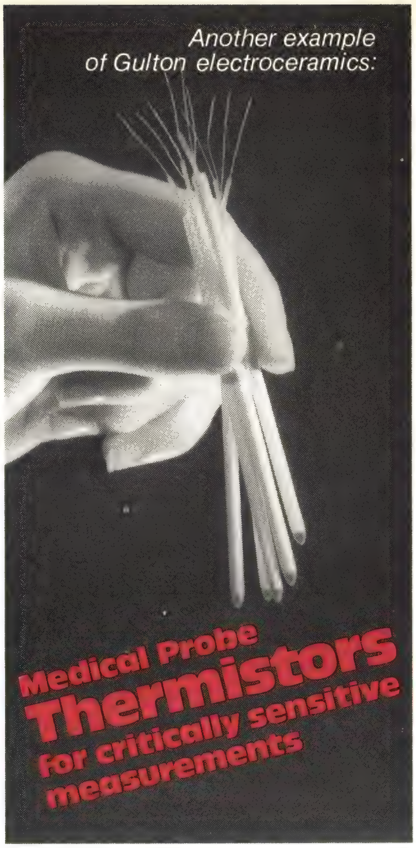
Another key precision-amp characteristic, low offset-voltage drift (TCV_{OS}), shows up impressively. For the 5507E, it is 0.7 μV/C, achieved by permanently altering an on-chip trimming network during factory test. No external components are required since frequency compensation and short-circuit protection are internal.

At 18 V/μs, the 5501's slew rate is 50% faster than the amplifier for which it substitutes, the OP-01. Since the 5501's primary function is to be a fast DAC follower, a higher slew rate enhances its capability. Even more important, perhaps, is the chip's settling time: 1.0 μs maximum, to 0.1% of a 5-V input. Internal frequency compensation assures stable, high-speed performance without using external capacitors.

In addition to serving as replacements for the OP05 and 07, the 5505 and 5507 are superior substitutes for general-purpose 741 op amps, and for instrumentation-quality amplifiers such as the 725 and 108A.

Pricing is \$3.20 for the 5505 and \$4.50 for the 5507, both in plastic mini-DIP and 100-quantities; \$11.80 for the 5510 in 14-pin plastic DIP and 100-quantities. Delivery is from stock at Micro Power Systems distributors.

CIRCLE NO. 308



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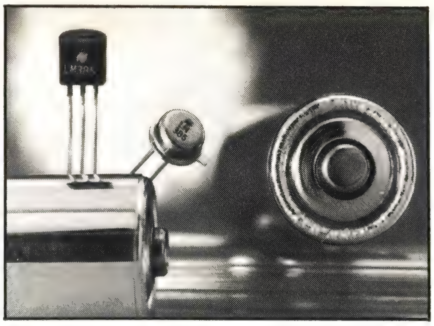
CIRCLE NUMBER 70

Two-terminal voltage references work down to 10 μA

National Semiconductor, 2900 Semiconductor Drive, Santa Clara, CA 95051. Dave Whetstone (408) 737-5000. P&A: See text.

The LM185 family of IC voltage references can operate with supply currents of just 10 μA—one-fifth that of competing references. These two-terminal devices have an operating range stretching to 20 mA, and deliver a reference voltage of 1.235 V with a 1 or 2% tolerance.



There are three basic versions: the LM185, 285 and 385. All three have a maximum reverse dynamic resistance of 1 Ω (at I_R = 100 μA), and a typical temperature coefficient of just 20 ppm/°C. The big distinction is the operating range: −55 to +125 C, −25 to +85 C, and 0 to 70 C, respectively.

Voltage stability over temperature holds to within 5 mV of the initial voltage, and wideband noise (over a 10-Hz to 10-kHz spectrum) is typically just 60 μV. The reference can also remain stable with capacitive loads—for reference currents below 1 mA, it can handle up to 1000 pF, and for higher operating currents, loads of several microfarads.

All three members come in a hermetic TO-46 metal package, with the LM385 also available in a low-cost TO-92 plastic package. Prices for the references start at just $1.20 for the plastic TO-92 version, the LM385Z, in 100-unit lots. Delivery is from stock.

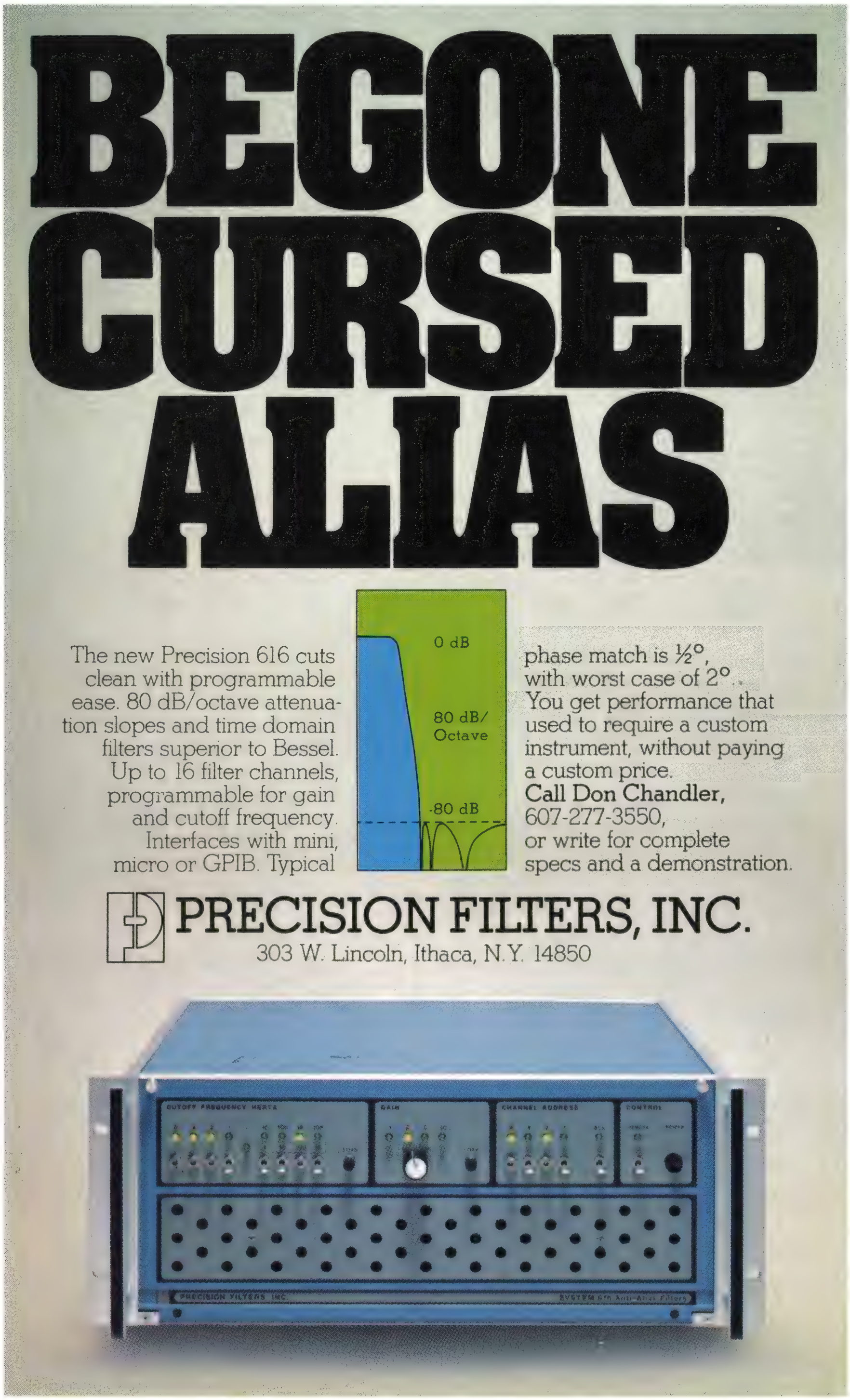
CIRCLE NO. 309

12-bit d/a converter updates at 50-MHz rate

ILC Data Device, Airport International Plaza, Bohemia, NY 11716. (516) 567-5600. From $595 (small qty).

A low-glitch, 12-bit d/a converter updates at a 50-MHz rate. The device offers 50-mA output current capability, 5000 m V-ns maximum glitch energy and a linearity error of only ±0.0125%. Settling time for a 1 LSB input change is 50 ns typical; for a full-scale input change, 400 ns typical. The TTL-compatible unit has a low-skew digital input register and an internal reference. Output voltage ranges are pin-programmable. No external components are required, except for optional offset and gain trim resistors. Voltage ranges are ±2.5, ±5, ±10, 0 to −5 and 0 to −10 V. Coding is binary or offset binary. Power requirement is ±15 and +5 V.

CIRCLE NO. 339



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CIRCLE NUMBER 71

Low-pass filter offers cut-off frequency choice

A.P. Circuit, 865 West End Ave., New York, New York 10025. (212) 222-0876.

Model AP-DP-8S-5P, a five-pole, 30 dB/octave low-pass filter, permits a choice of eight cut-off frequencies in the 10 Hz to 100-kHz range. Cut-off frequencies can be selected at from f_0 to $128f_0$. Response is maximum flatness Butterworth. An external switch converts response to a linearized phase type suitable for pulse work. The filter requires ±6 V at 17 mA. Input impedance is 20 kΩ; frequency stability, 0.005%/°C; frequency accuracy, ±5%. The filter measures 3.5 × 2.5 × 0.5 in.

CIRCLE NO. 340

Circuit monitors ac/dc line or load

Power Interface, 3350 Scott Blvd., Bldg. 34, Santa Clara, CA 95051. (408) 727-1991. $3.45 (1000 qty); stock.

A power monitor circuit, PM1100, reports on ac or dc line or load conditions. The information can be sent to control logic in a feedback loop. Two parallel-connected LEDs at the input accept ac or either polarity dc. An external resistor limits current for operation at voltages to 240 V ac. The output will source or sink up to 200 mA for direct operation with popular logic types. I/O isolation is 10^{11} Ω. The device comes in an 8-pin epoxy DIP.

CIRCLE NO. 341

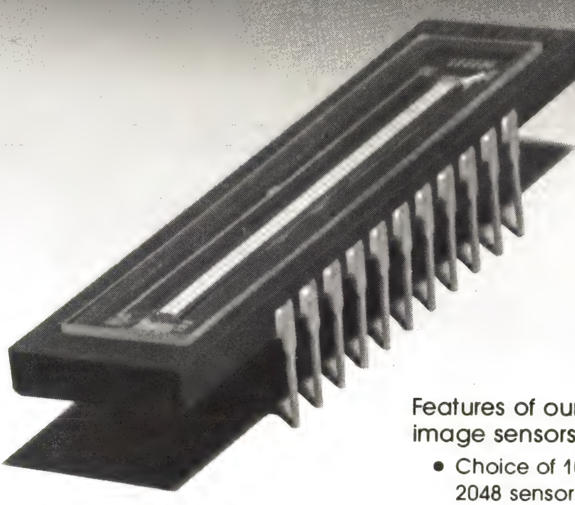
D/a subsystems settle in only 200 ns

Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. (408) 739-7700. $6.95 (plastic); $7.95 (ceramic) (100 qty).

Eight-digit d/a converters, NE/SE5118/9, settle in only 200 ns with 0.1% accuracy. Features include 10-μA data inputs, addressing capability and complying logic levels. The series provides a programmable current sink of from 0 to 2 mA and a timing requirement of less than 1 μs. Design includes internal feedback and input resistors for good thermal tracking characteristics and a short-circuit protected, on-chip, low-tempco voltage reference. Model 5118 offers ±0.19% accuracy; Model 5119, ±0.1% accuracy. Gain tempco is 5 ppm/°C for the 5118 and 20 ppm/°C for the 5119, independent of internal reference. Plastic or ceramic packages are available.

CIRCLE NO. 342

The Secret of Document Scanning is RETICON



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WHY? Because Design Engineers throughout the world have long recognized that using RETICON devices provides them with the latest, most advanced technology — the Secret of Success.

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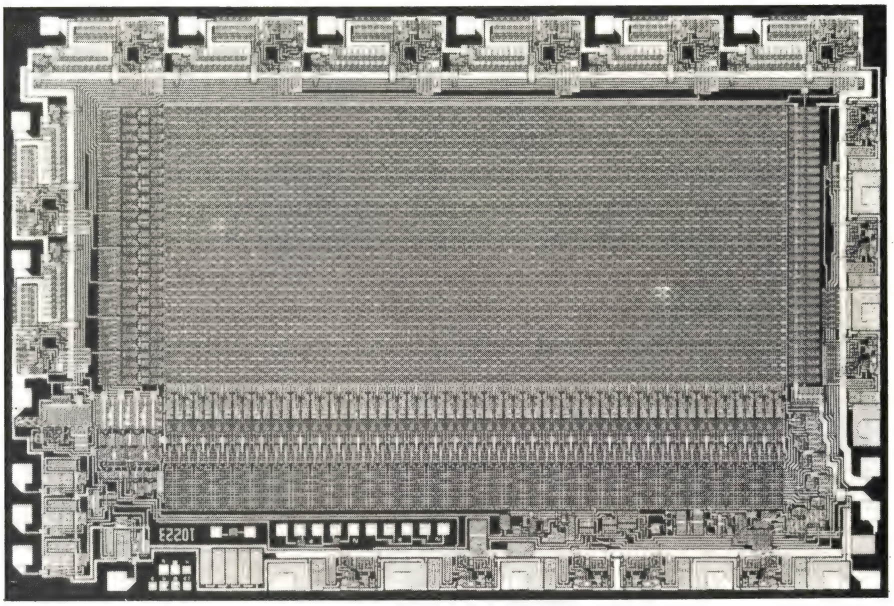
CIRCLE NUMBER 72

Fully static CMOS UV EPROM keeps power, parts count low



RCA, Solid State Div., Route 202, Somerville, NJ 08876. Jim Magos (201) 685-6717. P&A: See text; stock.

A CMOS fully static UV EPROM from RCA sports a storage capacity of 256 bytes and consumes just 50 μW when not being accessed (5 V at 10 μA). What's more, the CDP18U42 is fully compatible with RCA's CDP1800 microprocessor family, requiring no external components to interface with the CPU. And since the device is fully static (asynchronous) the address strobe signal has been eliminated.

With the CDP18U42, there are now two companies that offer CMOS UV EPROMs. Intersil (Cupertino, CA) offers the 6653 and 6654, whose respective storage capacities are 1 k × 4 and 512 × 8. Though these offer 1-μA standby mode current drain to the RCA device's 10 μA, the Intersil devices are synchronous devices.

Furthermore, the RCA unit operates at lower power levels during read cycles—just 20 mW, maximum, vs 30 mW for the Intersil devices. And where the CDP18U42 requires no external components, the Intersil circuits may need an external gate or two.

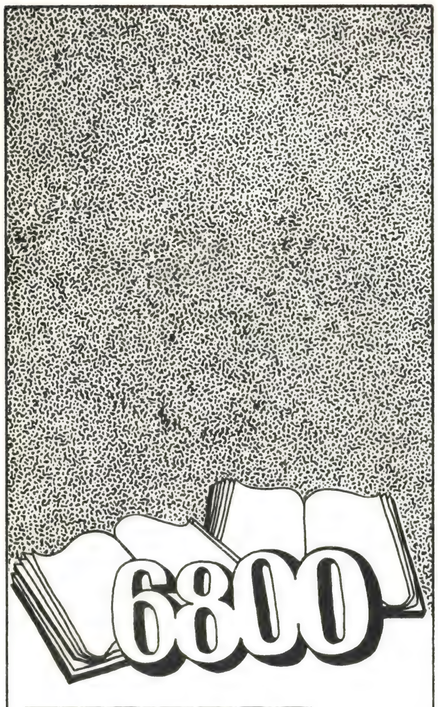
Maximum access time of the CDP18U42 is 1 μs, while the programming time is a reasonably fast 5 s. Although the unit can operate in the read mode with a nominal 5-V supply, the actual supply voltage can range from 4 to 6.5 V.

A functional replacement for the 1700 series UV EPROM, the CDP18U42 comes in a 24-pin, 600-mil-wide DIP and offers three-state, TTL-compatible output lines. Three chip-select lines can be used to enable the unit in large systems. Initially, all 2048 bits of the EPROM are in the ZERO state, and programming is done on a byte basis, where any erased bits can be selectively programmed to a ONE state at any address location or in any sequence.

Just the single program voltage (18 to 22 V) has to be used to pulse (10 ms, typical) the V_{DD} and V_{sat} lines simultaneously to program a byte. The data output terminals become true inputs, while the address inputs remain the same as in the read mode. Each memory location need only be programmed once, thus saving the necessity to cycle through the memory more than once.

Samples of the CDP18U42 are now available for $28.40 in 100-quantity lots. A 1-k × 8 version of the CMOS UV EPROM, compatible with the 2758-type single-supply NMOS units, is expected in the second half of 1980.

CIRCLE NO. 310



THE 6800 STORY IN TWO GUIDES IDEAL FOR HOBBYISTS

BASIC MICROPROCESSORS AND THE 6800 by Ron Bishop. Here is the first truly complete beginner's guide to microprocessors. It starts at ground zero with the basic fundamentals of microprocessors that must be mastered before any microcomputer system is learned. Then, it goes on to describe in detail the M6800 microcomputer system. Sample flowcharts and programs are found throughout, with extensive problem sections at the end of each chapter. #0758-2, paper, $12.90.

THE 6800 MICROPROCESSOR: A Self-Study Course with Applications, by Lance A. Leventhal. This is an ideal manual for hobbyists to gain hands-on experience with the 6800. Fifteen self-paced, increasingly complex laboratory exercises emphasize the use of the microcomputer as a controller. Flowcharts and examples are used throughout. #5120-4, paper, $8.60.

Available at your local computer store!

HAYDEN BOOK COMPANY, INC.
50 Essex Street, Rochelle Park, NJ 07662

CMOS watch circuit drives multiplexed LCDs

OKI Semiconductor, 1333 Lawrence Expressway, Santa Clara, CA 95051. (408) 984-4840. $5.95 (OEM qty).

A CMOS, multifunction digital watch circuit, MSM5081, drives multiplexed LCDs of eight digits, seven flags and 13 information indicators. The circuit provides time, date and day (in two time zones), a 1970 to 2009 calendar, two alarm modes, a stopwatch, a countdown timer and a selectable hourly chime. The circuit is available in die form suitable for hybrid assembly.

CIRCLE NO. 343

CMOS IC replaces software for μC timekeeping

NEC Electron, 3120 Central Expressway, Santa Clara, CA 95051. (408) 241-8222. $3.50 (1000 qty); stock.

A CMOS calendar and clock circuit, μPD-1990C, maintains time information, freeing its host computer for other tasks. The 14-pin device supplies timing pulse outputs at 64, 256 or 2048 Hz for input compatibility. Time setting and serial output follow a BCD format, except for month, which is hexadecimal. Reference frequency is generated by a crystal oscillator at 32.768 kHz. Operating voltage is 3.6 V with a maximum current draw of 100 μA. A 5-V version will be available in February 1980. Operating temperature range is −40 to 85 C.

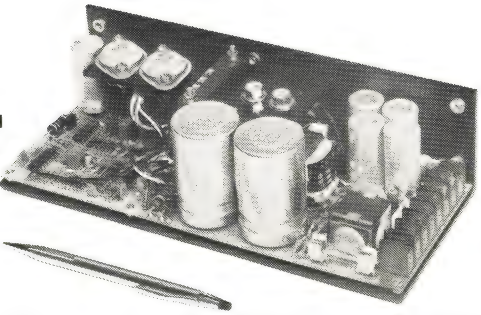
CIRCLE NO. 344

1-k ECL RAM performs with fast access times

Fujitsu America, 2945 Kifer Ave., Santa Clara, CA 95051. (408) 727-1700.

A 1024 × 1 ECL RAM, MBM 10415AH, translates small cell and chip sizes into very fast access times. Typical address access time is 12 ns (20 ns maximum). The memory is suitable for high-speed scratchpad, control and buffer storage memory. The device comes in a frit-sealed, 16-pin DIP. It is fully compatible with industry-standard 10-k series ECL families. Power dissipation is 0.5 mW/bit.

CIRCLE NO. 345



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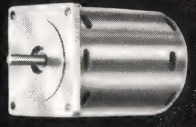
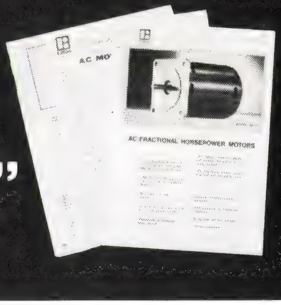
CIRCLE NUMBER 99





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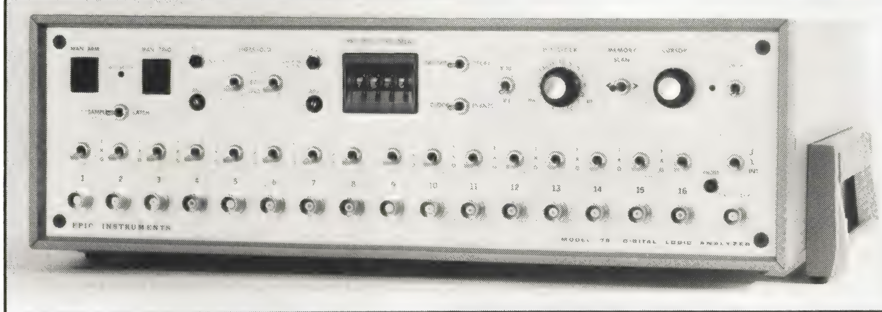
CIRCLE NUMBER 100

Logic analyzer offers most channels, memory for $2000



Epic Instruments Inc., 551-G Foster City Boulevard, Foster City, CA 94404. Bill Ballowe (415) 574-9081. P&A: See text.

For $2000, Epic Instruments' Model 78 logic analyzer offers much more than other comparably priced units: a 20-MHz clock, 16 channels of data-acquisition capability, each channel having 1024 bits of memory, and sophisticated display features.

Other analyzers in this price range, like the Biomation 920D, offer some of these features but not all. Most units supply 250 or 512-bit memories per channel and typically contain no more than eight or nine data-acquisition channels. And while a 20-MHz clock is not uncommon (Hewlett-Packard's 1620DA has one) some go only as high as 10 MHz.

Not only that, but the new analyzer's display can do single-step as well as circular scanning through memory. This means that even after reaching one extent of memory, the operator continues in the same direction, scanning out one end of the memory and immediately into the opposite end. With other units, the operator would have to scroll backward linearly through the memory to the opposite extreme of the memory.

In addition, single-step scanning makes it easy to count time. By beginning at the leading edge of a waveform and counting the single steps required to traverse the width of the pulse being measured, the operator can easily determine time by multiplying the external or internal clock period by the count.

Besides these features, the logic analyzer offers both pretrigger and posttrigger capability, which can be delayed or advanced by an operator-prescribed number of clock pulses. In addition, the unit can delay triggering by a specified number of trigger-event occurrences.

In pretrigger, after the specified number of events is counted, the analyzer stops recording with the last 1024 bits of each channel currently in memory. In posttrigger, triggering occurs once the prescribed number of events is counted. The next 1024 bits of memory are then recorded automatically by the analyzer.

The instrument also has some impressive input features, including a 10-ns minimum glitch-capturing ability. In addition, each channel offers a 1-MΩ input impedance and can tolerate a ±25-V input signal. All channels can be configured for TTL (+1.4 V), ECL (−1.3 V), or variable (±2.5-V) input threshold. Furthermore, channels 1 through 8 have separate threshold controls from 9 through 16 and clock for added flexibility.

Other display features include an intensified narrow dot that can help line up the data edges of the 16 channels. What's more, 1/10th-screen intensification helps indicate the portion of memory subject to ten-times horizontal expansion. And a 3-bit intensification is used to indicate the beginning of memory.

In single-unit quantities, the instrument sells for $2000. Delivery takes 30 days.

CIRCLE NO. 321

The AmZ8000 is cheaper, easier, and a whole lot faster to program than the 8086.

Call Advanced Micro Devices and get all the facts on the AmZ8000. It's the best 16-bit CPU there is.

Advanced Micro Devices

901 Thompson Place
Sunnyvale, CA 94086
Tel: (408) 732-2400

CIRCLE NUMBER 75

10-MHz scopes assist design work

B&K-Precision, 6460 W. Cortland St., Chicago, IL 60635. (312) 889-9087. $700 (1476); $560 (1466); stock.

Two 10-MHz oscilloscopes, the dual-trace Model 1476 and the single-trace Model 1466, assist general-purpose engineering design and troubleshooting. Eighteen sweep range selections are available from 1 μs/cm to 0.5 s/cm with sweep speeds to 0.2μs/cm at 5× magnification. Triggered and automatic sync are offered with 10 mV/cm sensitivity. Either scope can be used to check divider networks in systems using TTL, CMOS, DTL and most ECL logic. A TTL-compatible intensity modulation input is available for time markers and character displays. Model 1476 features front-panel vectorscope or X-Y operation with matched sensitivity inputs. Model 1466 allows vectorscope operation. Verical and horizontal sync separation circuits are built-in, permitting expansion of any portion of a complex video waveform.

CIRCLE NO. 346

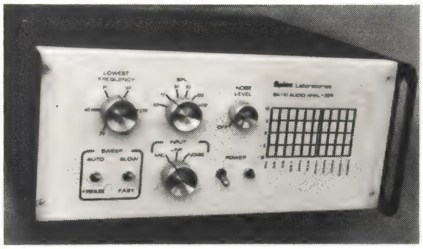
Low-cost substitution box switches in capacitance

Cincinnati Electrosystems, 469 Ward's Corner Rd., Loveland, OH 45140. (513) 831-4347. $20.95.

A low-cost capacitance substitution box switches in any of 21 capacitance values from 100 pF to 10 μF. The compact unit measures 4 × 2-7/8 × 1-9/16.

CIRCLE NO. 347

Spectrum analyzer offers 1/9-octave resolution



Spies Laboratories, P.O. Box 336, Lawndale, CA 90260. (213) 644-0056. $1195; 4 to 6 wks.

An audio spectrum analyzer, Model SA-91, offers 1/9-octave resolution. A single, voltage-controlled filter is swept over the audio range in 91 bands. Dynamic range of the display is 20 dB in 101 distinct 0.2-dB points. The instrument drives a television (through an rf modulator) or a video monitor. Microphone and line-level inputs are provided. Outputs are pink noise and composite video.

CIRCLE NO. 348

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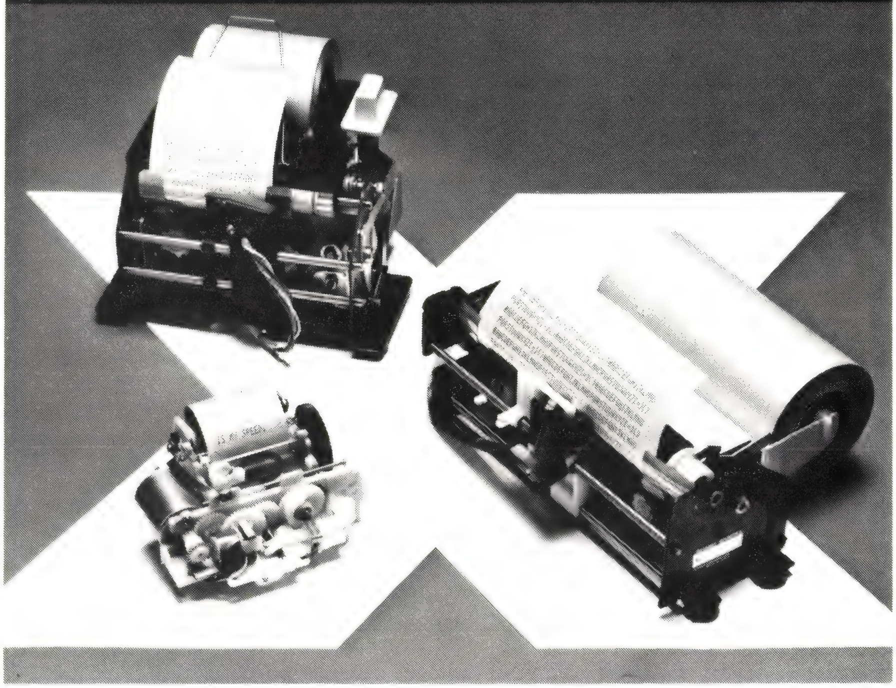

CIRCLE NUMBER 76

NEW PRODUCT
CHARGE SENSITIVE PREAMPLIFIERS

Models A-203 and A-206 are a Charge Sensitive Preamplifier/Pulse Shaper and a matching Voltage Amplifier/Discriminator developed especially for instrumentation employing solid state detectors, proportional counters, photomultipliers, channel electron mutipliers or any charge producing detectors in the pulse height analysis or pulse counting mode of operation.

These hybrid integrated circuits feature single supply voltage, low power dissipation (16mW), low noise, pole zero cancellation, unipolar and bipolar outputs and adjustable discrimination level.

All Amptek, Inc., products have a one year warranty.

Model A-101 is a Charge Sensitive Preamplifier-Discriminator and Pulse Shaper developed especially for instrumentation employing photomultipliers, channel electron multipliers and other charge producing detectors in the pulse counting mode. Its small size (TO-8 package) allows mounting close to the collector of the multiplier. Power is typically 15 milliwatts and output interfaces directly with C-MOS and TTL logic. Input threshold and output pulse width are externally adjustable.

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CIRCLE NUMBER 77

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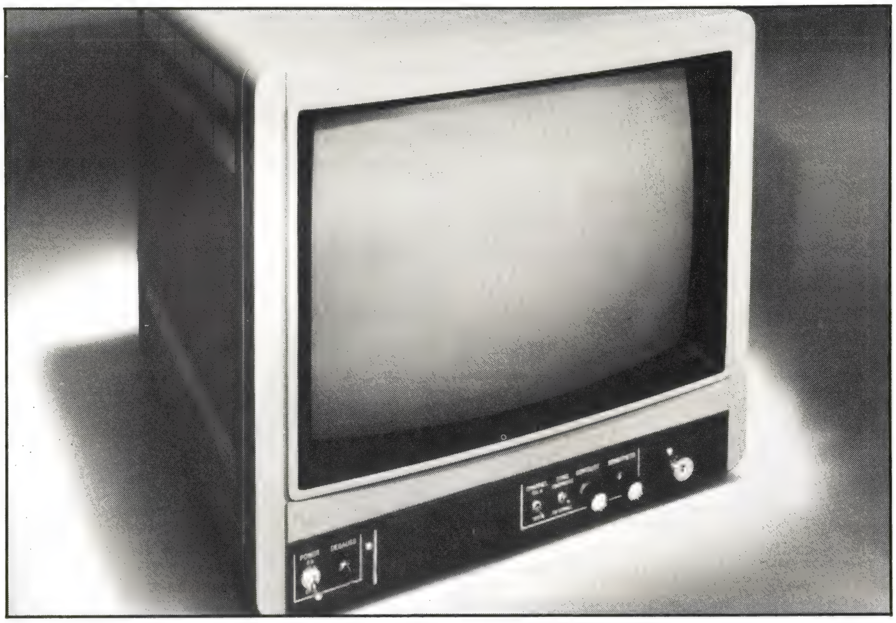
CIRCLE NUMBER 78

$2000 color monitor offers high resolution, dot pitch



Hitachi America, Ltd., 100 California St., San Francisco, CA 94111. Kazuo (Ken) Takei (415) 981-7871. P&A: See text.

Using a dot-matrix IC and a unitized, in-line high-resolution gun, a color monitor in the $2000 range offers a resolution of 1280 horizontal and 960 vertical dot triads on a 19-in. screen. What's more, each dot triad sports a 0.31-mm dot pitch—almost twice as good as the pitch normally offered in this price range.

Two versions are being offered by Hitachi America: the HM-2619 19-in. and HM-2613 13-in. for rugged industrial applications, with even less expensive counterparts, the HM-2719 and HM-2713, for commercial-grade applications.

High resolution stems from the combination of 0.31-mm dot pitch and unitized in-line, high-resolution gun, which is used instead of a common gun array. The in-line gun needs no complicated convergence circuits—or the recurring readjustment these circuits require.

What little convergence readjustment is required is handled by double-deflection coils on the monitor. Misconvergence is reportedly less than 0.5 mm within a circle whose diameter is equal to the vertical height of the display. Outside the circle's perimeter, misconvergence rises to 1.0 mm.

What's more, while other 13-in. monitors have in-line gun configurations, the HM-2719 is the only 19-in. monitor offering such an improvement.

Other technology improvements abound. For example, while other monitors typically operate with a bandwidth that ranges from 50 Hz to at most 15 MHz, the Hitachi product goes from 50 Hz to 25 MHz ±3 dB. This performance fills a gap between the low and ultrahigh-resolution monitors.

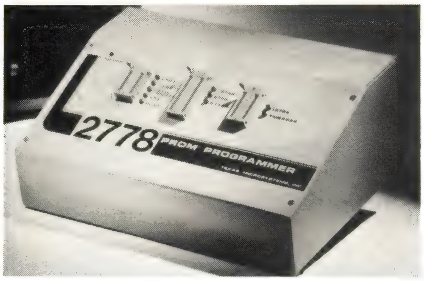
Display flickering is not a problem. Instead of higher refresh rate, phosphor is used whose persistence is long enough to prevent flickering but short enough not to create ghosts as the screen's image changes.

In addition, the monitor offers 15 to 18-kHz line frequency, 10-μs horizontal retrace, and 50 or 60-Hz interlaced refresh. The monitor also can be operated in a noninterlaced mode.

The HM-2619 sells for $2400, the 2613 for $2000; the HM-2719 sells for $1900, the 2713 for $1400—all in 100-unit quantities. All are available 90 days after order.

CIRCLE NO. 322

Programmer operates with Intellec MDS

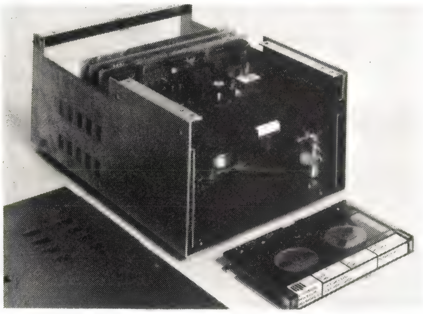


Texas Microsystems, 10503 Rockley Rd., Suite 108, Houston, TX 77099. (713) 933-7503. $1295; 4 to 6 wks.

An EPROM programmer, Model 2778, handles a variety of popular types without the need for personality modules. Operation is through the Intellec microcomputer development system, using software provided with the programmer. Devices which can be programmed include the 2708, TMS2716, Intel 2716/TMS2516, Intel 2732, TMS2532, 8741A, 8748, 8755A, TMS2564, Intel 2764 and Motorola MCM 68764. Device types are easily changed with a plug and socket arrangement. Software is provided on single and double diskette formats.

CIRCLE NO. 349

Cartridge drive allows OEM formatting options



Electronic Processors, 1265 W. Dartmouth Ave., Englewood, CO 80110. (303) 761-8540. Approx. $700 (OEM qty); 8 wks.

Model STR-810, a digital recorder using DC-300A cartridges, allows user choice of formatting, tape speeds and read/write heads with from one to four tracks. OEMs can determine data rate, packing density and formats, limited only by the bandwidth of the read/write head. The only moving part is the cartridge engagement cam. Under microprocessor control, STR-810 monitors its own tape movement, relieving a host CPU from the responsibility. Capacity per 300-ft cartridge is 23 Mbits of unformatted data. The unit measures 5.2 × 7.8 × 12.75 in.

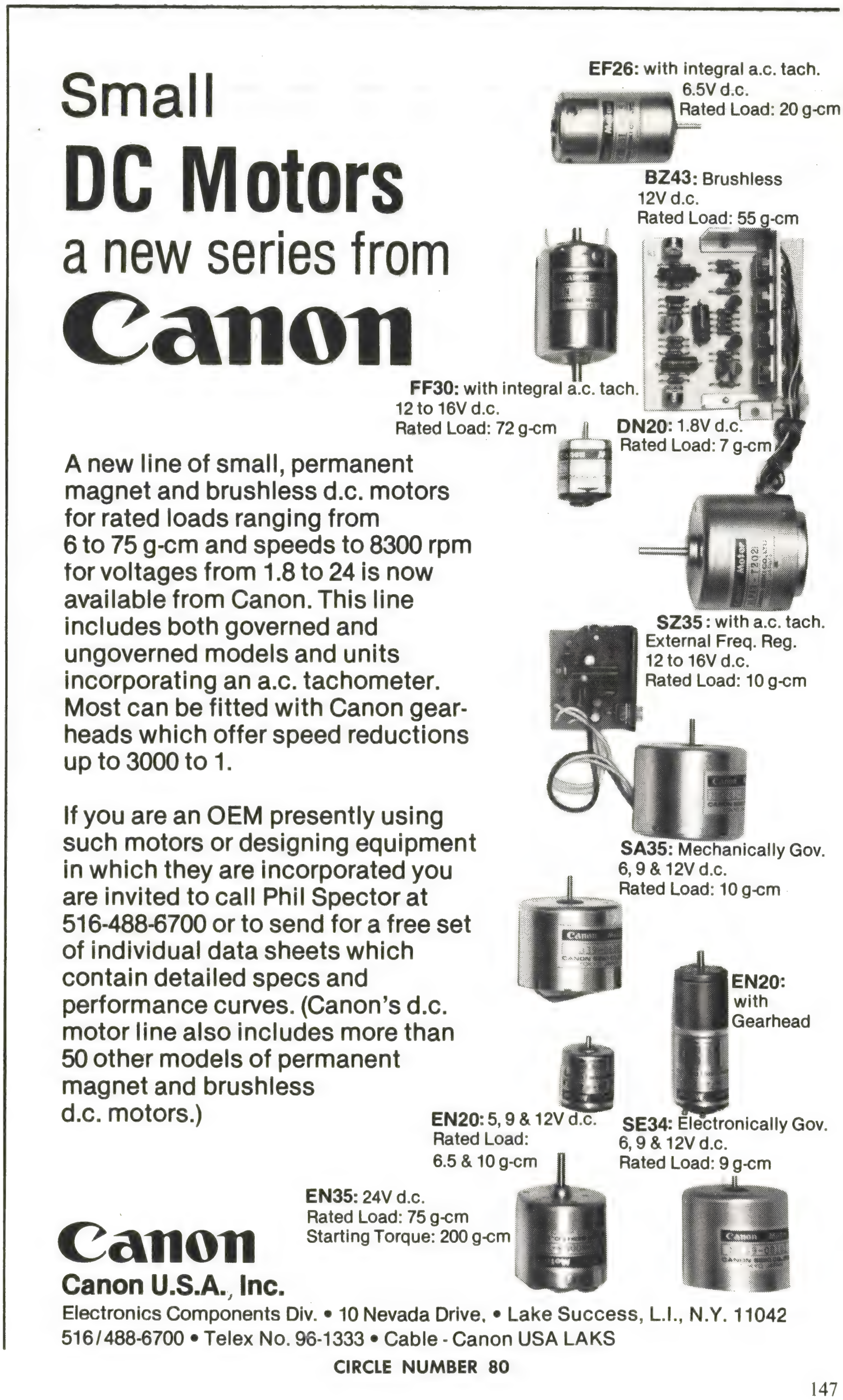
CIRCLE NO. 354

Impact printer ties into mini/microcomputers

Durant Digital Instruments, 901 S. 12th St., Watertown, WI 53094. (414) 261-4070. $645; stock.

A free-standing impact printer, System 6070, ties into a broad range of mini and micrcomputers. The 5 × 7 dot matrix unit comes with built-in serial asynchronous interfaces and parallel 7-bit ASCII and BCD interfaces. Serial interfaces offer simple connection to computer teletypewriter or RS232C outputs. System 6070 uses conventional adding machine paper. An ac synchronous motor controls printhead motion, paper advance, ribbon feed and automatic ribbon reversing. Average printing rate is 40 characters/s. The printer measures 6 × 10-1/2 × 14 in.

CIRCLE NO. 355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A new line of small, permanent magnet and brushless d.c. motors for rated loads ranging from 6 to 75 g-cm and speeds to 8300 rpm for voltages from 1.8 to 24 is now available from Canon. This line includes both governed and ungoverned models and units incorporating an a.c. tachometer. Most can be fitted with Canon gearheads which offer speed reductions up to 3000 to 1.

If you are an OEM presently using such motors or designing equipment in which they are incorporated you are invited to call Phil Spector at 516-488-6700 or to send for a free set of individual data sheets which contain detailed specs and performance curves. (Canon's d.c. motor line also includes more than 50 other models of permanent magnet and brushless d.c. motors.)

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12 to 16V d.c.
Rated Load: 10 g-cm

SA35: Mechanically Gov.
6, 9 & 12V d.c.
Rated Load: 10 g-cm

EN20: with Gearhead

EN20: 5, 9 & 12V d.c.
Rated Load:
6.5 & 10 g-cm

SE34: Electronically Gov.
6, 9 & 12V d.c.
Rated Load: 9 g-cm

EN35: 24V d.c.
Rated Load: 75 g-cm
Starting Torque: 200 g-cm

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CIRCLE NUMBER 80

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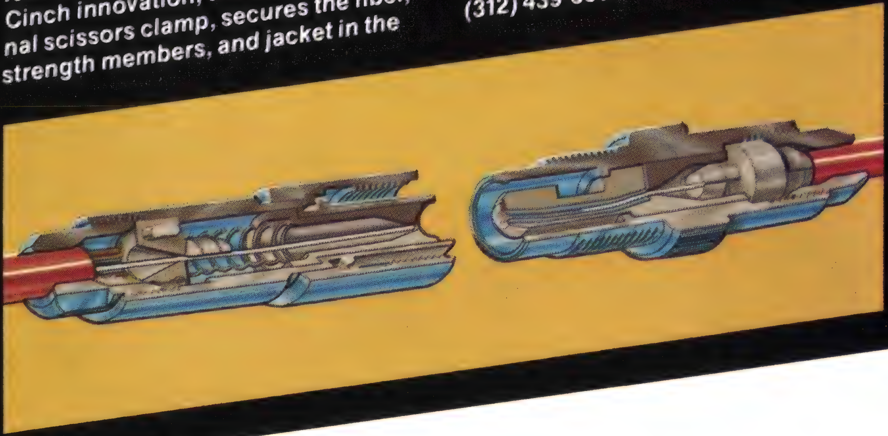
Compact OPTALIGN plugs and receptacles are ideal for computers, CATV, telecommunications, medical, instrumentation and military applications. Dimensions are ⅝" diameter x 1½" in length.

If you require a miniature single-fiber optic coupling, we've got that too. It's our new Light Line* SMA Connector, another innovative, high-value offering from TRW Cinch.

These are just two new products from the new Cinch. We'll think "Innovation" when it comes to meeting your connector challenges, too! Call your TRW Electronic Components Sales Office . . . listed in EEM. TRW Cinch Connectors, A Division of TRW Inc., 1501 Morse Avenue, Elk Grove Village, IL 60007. (312) 439-8800.



the challenge innovation.

TRW CINCH CONNECTORS

"See Us at Nepcon West Booth No. 1021"

CIRCLE NUMBER 79

10.4-Mbyte data storage

Digital Equipment, 129 Parker St., Maynard, MA 01754. (617) 897-5111. $6900.

A 10.4-Mbyte cartridge disk drive, RL02, stores data for PDP-11 based minicomputer systems, PDP-11/03L and PDP-11/23 microcomputer subsystem configuration consists of a disk drive and controller. Up to three additional drives can be supported by the controller. Maximum storage capacity for an R*m*02 configuration is more than 83 Mbytes. A universal power supply permits 120 or 240-V ac operation.

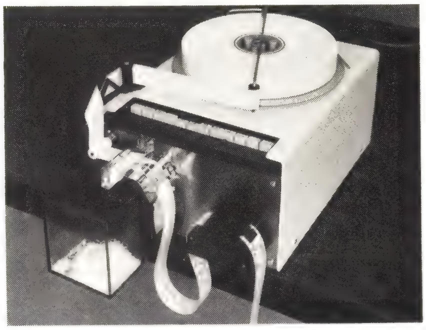
CIRCLE NO. 356

Informer, 8332 Osage Ave., Los Angeles, CA 90045. (213) 649-2030. $1170 (100 qty); stock to 6 wks.

A 19-in. rack-mount computer terminal, R301, requires only 7-in. of panel space. The unit comes with a 6-in. diagonal display monitor, a full alphanumeric keyboard, logic and power supply. Full or half-duplex operation is possible with transmission rates from 110 to 9600 baud. Interfaces are RS232 or 20 mA. Standard display format is 32 columns and 16 lines; 64 columns and 16 lines is also available. The keyboard can be removed from the panel and used up to 8 ft from the terminal. Power consumption is 100 W from a 90 to 250 V, 50/60-Hz supply.

CIRCLE NO. 357

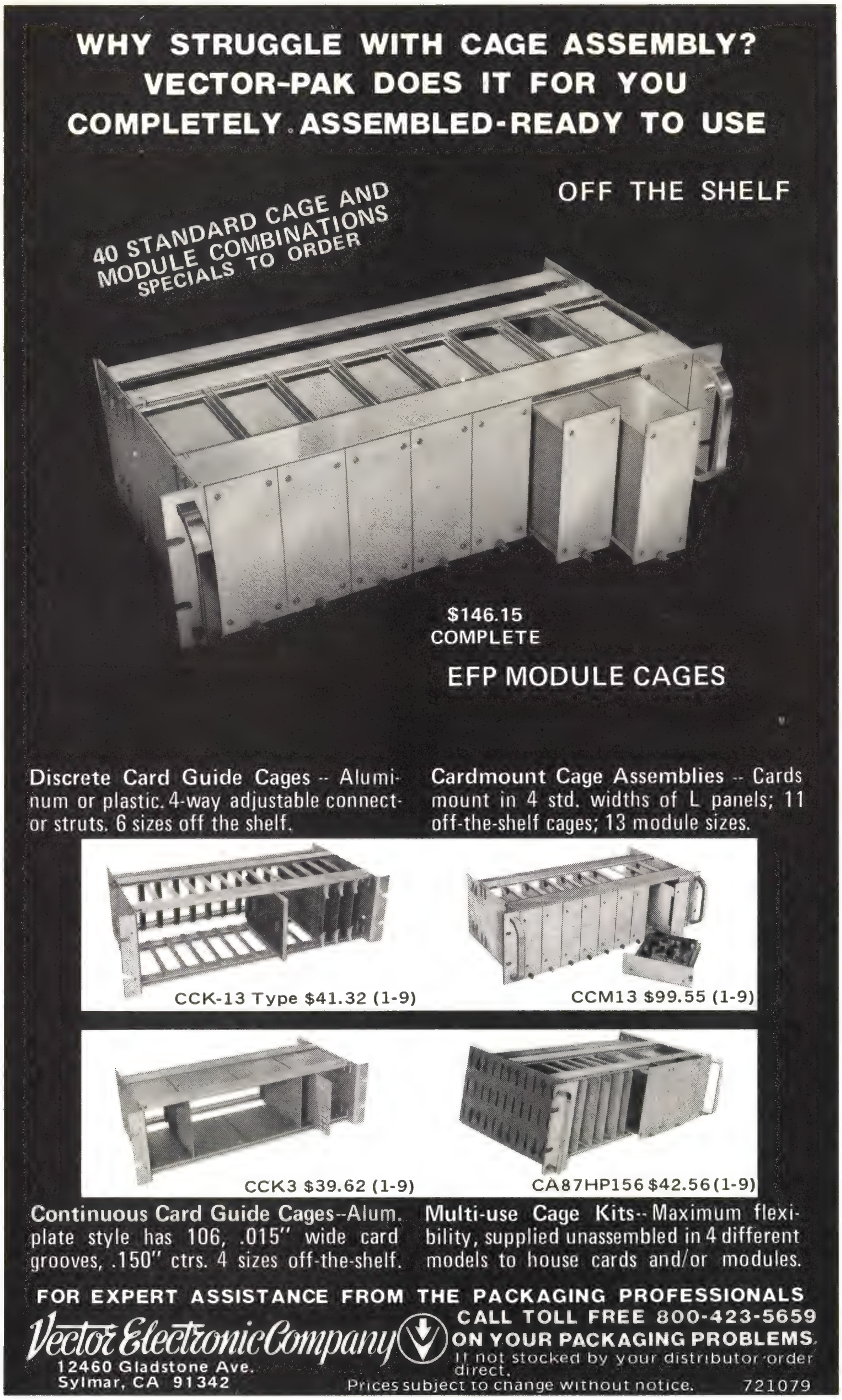
Paper punch/reader works under μP control



Drillick LaManna, 280 Midland Ave., Saddle Brook, NJ 07662. (201) 791-1414.

Guided by a TI 9981 microprocessor, the Model 18 paper tape terminal operates at up to 300 baud (30 char/s). The unit connects to a KSR printer, such as the Teletype Model 43 or DEC Model 34, for automatic send/receive capability. The terminal is equipped with dual ports with RS232C or CCITT V24 interfaces. Options include current loop interfaces, five-level operation for Telex and private wire circuits, answerback, 4 to 12-k buffer, code conversion and editing capabilities. The Model 18 punches Mylar, as well as paper tape and can sense a low tape supply.

CIRCLE NO. 358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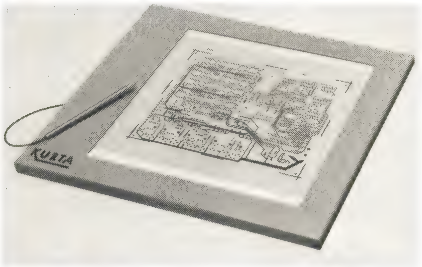
Sylmar, CA 91342

Prices subject to change without notice. 721079

CIRCLE NUMBER 81

Digitizer inputs graphics at real-time speeds

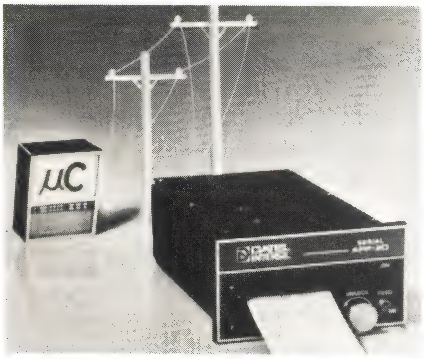


Kurta, 2202 S. Priest, Building 102, Tempe, AZ 85282. (602) 968-8709.

A graphics digitizer, with an 11 × 11-in. drawing area, provides a high-speed, contiguous data output. Real-time response is fast enough for writing and drawing applications. Resolutions of 100, 200 or 400 points/in. are available at a variable output rate of up to 2000 points/s.

CIRCLE NO. 359

Mini thermal printer needs only 2-wire hookup



Datel-Intersil, 11 Cabot Blvd., Mansfield, MA 02048. (617) 828-8000. $880; 2 to 8 wks.

A miniature, 20-column thermal printer, Model APP-20A2, needs only two wires to interface. All electronics, including a microprocessor, are contained inside the printer housing; no extra electronics are required. The unit prints up to 96 ASCII alphanumeric data characters at up to 1.2 lines/s. Although only two pins are needed to operate the printer, optional pin functions are available via a rear connector. Isolated TTY current loop input or standard RS232C connections are offered. Inverted printing is possible for text applications where the last line appears at the bottom of a printout, like a teletypewriter. Single-character printing is available for keyboard echo applications. The printer measures 8 × 2.76 × 4.44 in. and fits a 4.5 × 2.78-in. panel cutout.

CIRCLE NO. 360

Disk systems expand HP 3000 data storage

Microcomputer Systems, 432 Lakeside Dr., Sunnyvale, CA 94086. (408) 733-4200. Typical $23,500; 8 to 13 wks.

Two disk systems, based on MSC 1694 and 1696 disk controllers, increase the storage capacity of HP 3000 computers. The MSC 1694 controller handles up to eight disk drives with up to 300 Mbyte capacity. The MSC 1696 handles up to eight 600-Mbyte drives. Since the systems permit greater capacity with fewer drives, system costs for power, cooling and floor space can be reduced. The controllers allow expansion to 2 Gbytes (1694) or 4 Gbytes (1696). No change in operating system software is required to HP 3000 computers for addition of the MSC controllers which emulate HP 7925 drives. Each disk storage system includes a controller, a host adapter and up to eight disk drives. The host adapter, a single PC board, plugs directly into an HP 3000 selector channel to obtain emulation signals.

CIRCLE NO. 361

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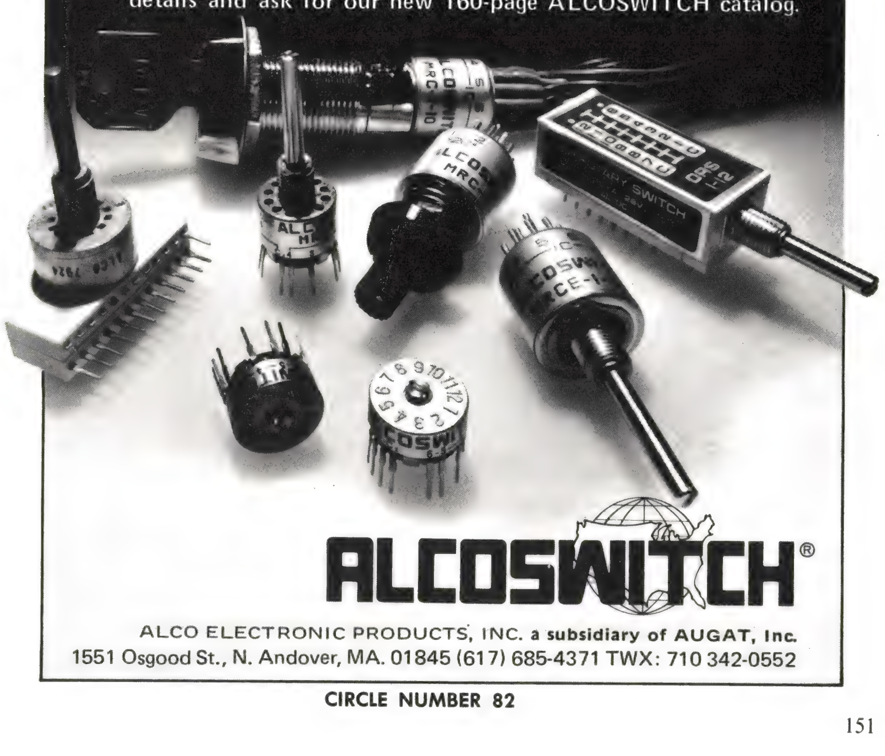

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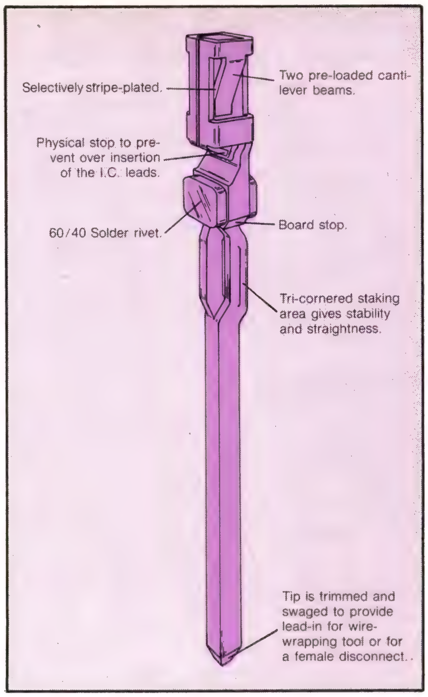
1551 Osgood St., N. Andover, MA. 01845 (617) 685-4371 TWX: 710 342-0552

CIRCLE NUMBER 82

Three-corner socket joins ICs to wire-wrapped connections

Berg Electronics, Div. of E.I. duPont de Nemours & Co., New Cumberland, PA 17070. Dick Vukmanic (717) 780-2010. P&A: See text.

In a single connector package, the Tri-Socket from Berg takes care of a multitude of functions: ICs can be plugged-in above the board, wire-wrapped connections can be made below. A novel tricornered compliant pin design allows the connector to be pressed into a plated-through hole, while a predeposited solder rivet accommodates soldering to above-board contact pads with reflow-soldering baths.


Selectively stripe-plated.
Two pre-loaded cantilever beams.
Physical stop to prevent over insertion of the I.C. leads.
60/40 Solder rivet.
Board stop.
Tri-cornered staking area gives stability and straightness.
Tip is trimmed and swaged to provide lead-in for wire-wrapping tool or for a female disconnect.

The versatile socket is made of a single piece of full-hard copper-nickel, with selective plating of 15 μin. of gold over 50 μin. of nickel. The top portion of the connector consists of two preloaded (folded) cantilever beams designed to provide tight edge contact with a large variety of IC pin sizes.

The tricornered stacking area, a variation of the compliant-pin approach, will allow the Tri-Socket connector to be press-fit into a plated-through hole using bench or hand tooling (although automated equipment can insert strips of pins at faster than 12,000 insertions per hour). A 60/40 solder rivet, precisely positioned above the tricornered staking area, enables the socket to be connected to PC-board pads using hot-oil submersion, infrared, or condensation vapor techniques. After reflow, Tri-Socket retention force is 60 lb.

The tip of the Tri-Socket connector is trimmed and swaged to provide an easy lead-in for a hand-held wire-wrapping tool or for a female disconnect socket.

The square pin below the board is available in several lengths up to 0.680 in. for wirewrapping. The Tri-Socket is available on strips and reels for machine insertion. The Tri-Socket connector can be inserted on 0.100-in. centers with a variety of insertion equipment ranging from simple hand tools to a computer-controlled positioning system. Price is approx. four to seven cents a line. Delivery is 4 to 8 weeks.

CIRCLE NO. 323

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RF communication is only as good as the antenna that receives your signal, so why gamble? Go with a proven antenna. In our 37 years we've gained a well-earned reputation for producing a wide-range of reliable, high performance airborne antennas: stubs, horns, blades, spirals, you name it and you'll find it in our new 80 page antenna catalog. Contact your local rep for your copy. And if you want to talk about unique requirements, call us.

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TPI

CIRCLE NUMBER 83

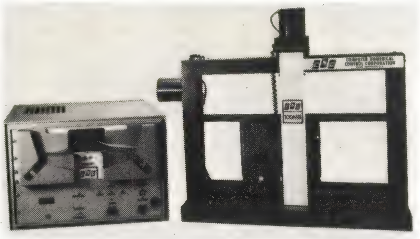
Sputtercoater metallizes CRT faceplates and LCDs

Varian Associates Vacuum Div., 611 Hansen Way, Palo Alto, CA 94303. (415) 493-4000.

A medium-sized sputtercoating system, ICS-50, coats the inside of CRT faceplates and LCD panels. Thin films of pure metals, alloys, metallic oxides and some non-metals can be vacuum-deposited onto plastics, glass, metals and many other prepared substrate surfaces. The coater works continually under vacuum; there is no need to stop the system to feed new parts. A microprocessor-based controller monitors and manages system operation. Unlike some techniques, sputtering produces no pollutants and can deposit metals and alloys on practically any surface.

CIRCLE NO. 362

Benchtop wirewrapper performs under PDP-11



Computer Numerical Control, 460 New Boston Park, Woburn, MA 01801. (617) 933-0091. $5995.

A benchtop wirewrapping system, the Mini-Brute CNC-100MB, interfaces to a DEC PDP-11 computer for R&D or production work. Wirewrapping area is 12 × 16 in. The unit is adaptable for insulation-displacement wiring.

CIRCLE NO. 363

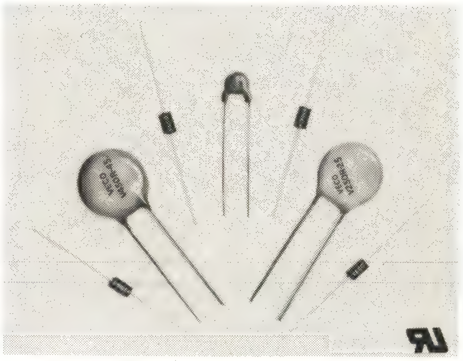
Selective gold plating lowers connector

Viking Connectors, 21001 Nordhoff St., Chatsworth, CA 91311, (213) 341-4330. Typical $3.50 (1000 qty). Stock to 9 wks.

Plating gold on contacts only in the area where they mate with PC boards helps lower the cost of a varied line of connectors. Tin plating is used on areas outside of the selective gold area. One version comes with from 8 to 70 contact positions on a 0.1 × 0.2-in. grid. Another has from 6 to 50 contact positions on a 0.125 × 0.25-in. grid. Wire-wrap, solder and right-angle tail configurations are offered. Mounting flanges and polarization keying are available.

CIRCLE NO. 364

METAL OXIDE VARISTORS from VECO Lower System Costs



Victory's new metal oxide varistors are designed to lower system costs and increase product safety through improved circuit and system reliability. It is very important to note that the published energy rating expressed in joules is after the application of 2000 pulses, where as many competitive devices are rated at only one pulse.

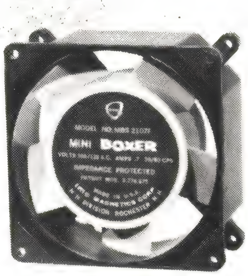
Veco metal oxide varistors exhibit improved response times, increased current capability, low standby power consumption and superior clamping characteristics in a compact, lightweight package that's UL recognized for "across-the-line" components.

VICTORY ENGINEERING CORP.
Victory Road, P.O. Box 599, Springfield, NJ 07081
(201) 379-5900 TWX: 710-983-4430

CIRCLE NUMBER 84

for best results... first convert to IMC

IMC MINI BOXER FAN



When it comes to applications, IMC's Mini-Boxer Fan meets a large variety of uses—ranging from cash registers to tape decks. Variations of this model include the Ball Bearing, Grand Prix Sleeve Bearing, Skeleton and Mil Type Mini-Boxers—all with similar low profile applications. Literature on request! For further information please call Stan Barbas, Sales Manager at 603/332-5300 or write:

IMC MAGNETICS CORP.
NEW HAMPSHIRE DIVISION
ROUTE 16B, ROCHESTER, NEW HAMPSHIRE 03867

CIRCLE NUMBER 85

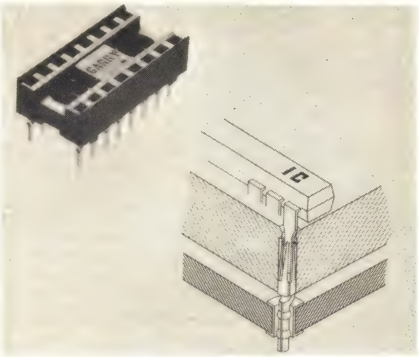
Rosin-free flux ends residue removal problems

Multicore Solders, S. Service Rd., Westbury, NY 11590. (516) 334-7450.

A rosin-free flux material, XERSIN, will, in most cases, eliminate the need to remove flux residues after soldering operations. The residues of XERSIN are less corrosive than those of rosin fluxes. Fumes given off during soldering are reduced. The material passes the Copper Mirror Test and performance requirements specified in QQ-P-571. It also passes MIL-P-28809 cleanliness tests. XERSIN is offered in wire-cored solder, as a liquid flux, including foaming types, and will soon be available in solder creams.

CIRCLE NO. 365

Four-tine contacts grip IC leads on all sides



Garry Manufacturing, 1010 Jersey Ave., New Brunswick, NJ 08902. (201) 545-2424. $0.02 to $0.04/contact; stock to 4 wks.

A series of wire-wrappable IC sockets, Series QS520/QS530, uses four-tine contacts to securely grip IC leads. The beryllium-copper Quad-Spring contacts surround an IC lead on all four sides, making contact with the face and edge of the pins at the same time. Quad-Spring contacts are offered in a closed-entry socket of thermoplastic or high-temperature diallyl phthalate FS-10 material. Contacts are gold or tin-plated. Sockets with from 8 to 40 contacts are available in 0.3 and 0.6-in. spacing.

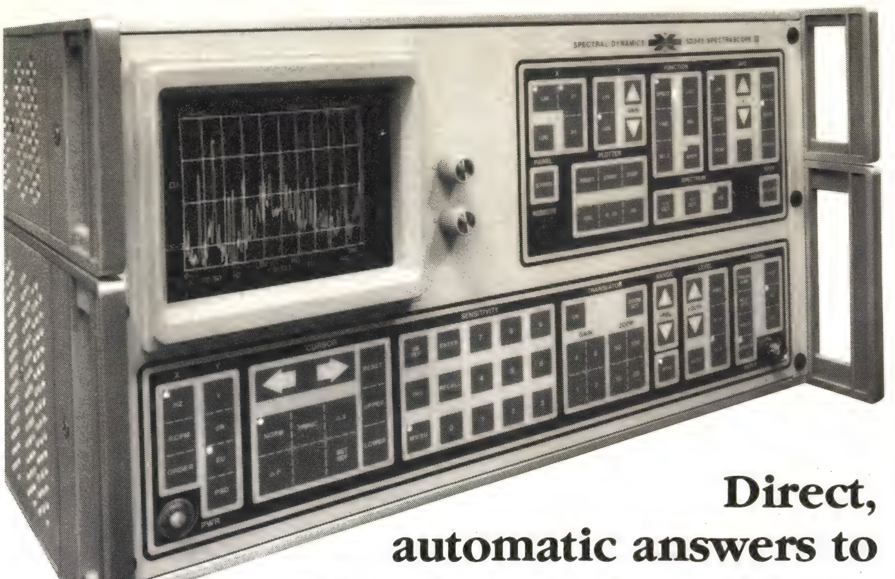
CIRCLE NO. 366

Positive-resist boards simplify circuit building

Vector Electronic, 12460 Gladstone Ave., Sylmar, CA 91342. (213) 365-9661. P&A: See text.

A five-component system quickly prepares custom circuit boards for S-100 bus systems. Key to the process is a positive resist-coated, double-sided copper-clad board, Model 8800R2. The 5.3 × 10-in. G10 board has 100 gold-flashed, nickel-plated card-edge contacts on 0.125-in. centers. To fabricate a board, a designer implements a circuit using R407 rub-transfer artwork on Mylar film. The Mylar is placed over a sensitized board and exposed to UV light or sunlight. Developer fixes exposed images. Etching is accomplished in a heavy plastic bag. Boards are $19.95; R407 artwork kits, $2.65; 2594F ferric-chloride etchant, $1.69; 2594A ammonium persulfate etchant, $1.30; 0088-21-45 developer, $2.46. All items are available from stock.

CIRCLE NO. 367

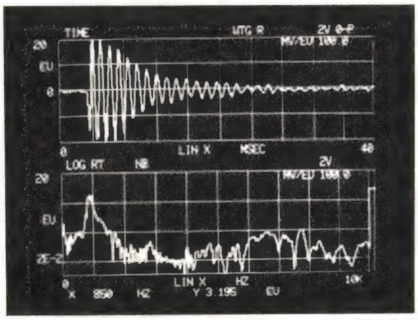


Direct, automatic answers to signal analysis problems . . . without calculations!

Confused by having to convert dB reference numbers to meaningful engineering unit (EU) values you can understand? The SD345 FFT Signal Analyzer does it automatically and displays the correct numbers instantly and directly on an exceptionally clear raster-scan display. Or you can record the answers by photography, digital or analog plotter, or video hard copy.

But getting instant, automatic solutions to your problems is only the first-order reason you should own the SD345. Our new 12-page brochure outlines its many other exclusive capabilities and applications. The SD345 is today's best buy . . . it's available right now . . . and we'll be glad to stage a live demonstration in your lab.

Call Leon Corcoran at (714) 268-7197 to schedule your demo.



Actual photo of raster scan display — flicker-free, with full grids, complete annotation and engineering-unit readouts for total answers, understandable and usable at a glance. An incoming time waveform can be displayed simultaneously with a spectrum analysis of that waveform (on a real time or averaged basis) for direct comparison.

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Scientific-Atlanta
P.O. Box 671 • San Diego, CA 92112 • (714) 268-7100 • TWX 910-335-2022

CIRCLE NUMBER 86

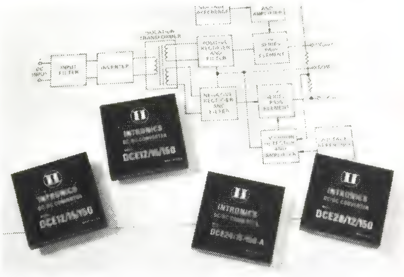
LCD system includes drive, refresh and power

Kylex, 420 Bernardo Ave., Mountain View, CA 94043. (415) 969-5200. $199 (100 qty); 6 wks.

A one-line, 40-character, 5 × 10 dot matrix LCD system, LX140, includes all electronics for direct microprocessor interface. The flat display panel is a low-voltage (5-V), low-power system with integral drive, refresh, temperature compensation and power supply electronics. Display capability includes the full ASCII character set, including lower case descenders and underline. On-board electronics includes CMOS drive chips with integral RAM for all 2000 display elements. Each dot is addressable. All I/O lines are compatible with 5-V logic families. Power drain is typically less than 400 mW. A 20-pin socket connector allows easy interface to a user's system.

CIRCLE NO. 368

Modular dc/dc converters put out ±12 and ±15 V

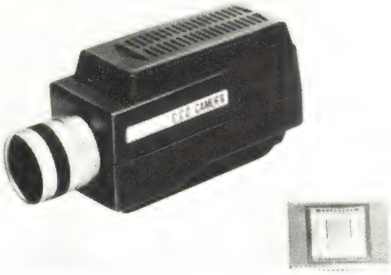


Intronics, 57 Chapel St., Newton, MA 02158. (617) 332-7350. $61; stock to 6 wks.

DCE Series dc/dc converters satisfy on-board need for low-noise ±12 and ±15 V power. All units offer output regulation of 0.02% maximum and only 1-mV rms noise. A high-attenuation input filter reduces kickback spikes, noise and reflected ripple caused by inverter switching. I/O isolation impedance is $10^9\Omega$; voltage isolation, 300 V dc. Eight models are available with inputs of 5, 12, 15, 24 and 28 V dc. Output current is 150 mA. The units operate under full load in a temperature range of −25 to +71 C. Size is 2 × 2 × 0.38 in.

CIRCLE NO. 369

Camera uses CCD chip for high-resolution video



Panasonic, One Panasonic Way, Secaucus, NJ 07094. Bill Bottari (201) 348-7276. Stock to 8 wks.

A monochrome, solid-state camera, BS-702, uses a charge-coupled device (CCD) for high-resolution video. The CCD chip provides 350 vertical lines and 360 horizontal lines. The chip has 248,832 pixels in its 512 × 468 matrix. The camera, without lens, weighs 540 g and measures 64 × 84 × 149 mm. Power consumption is 4.7 W.

CIRCLE NO. 370

EXPANDO

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241 Welsh Pool Road
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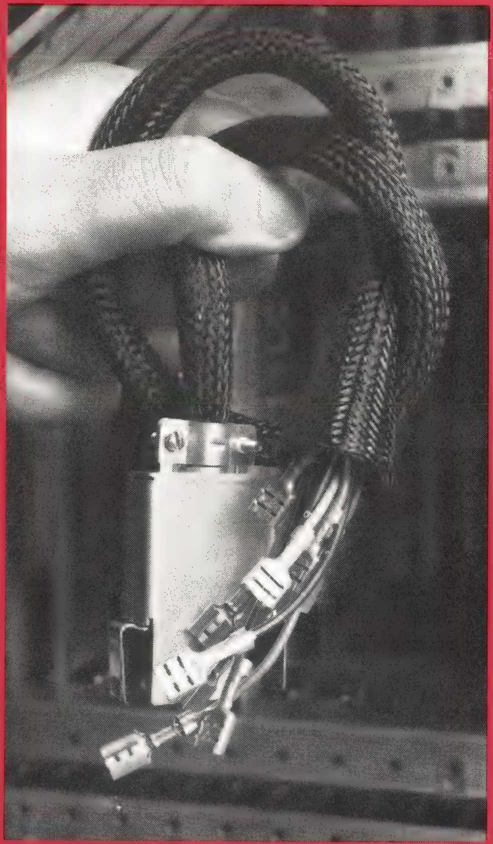
BentleyHarris

CIRCLE NUMBER 87



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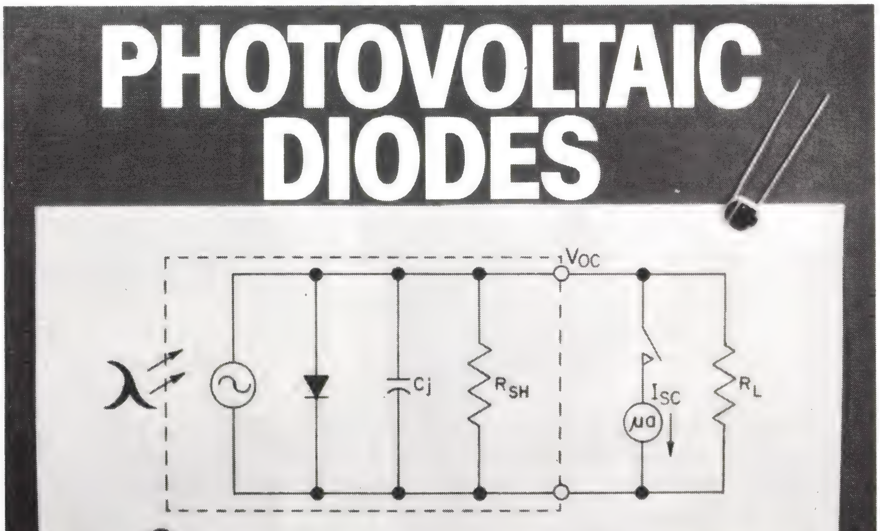
CIRCLE NUMBER 88



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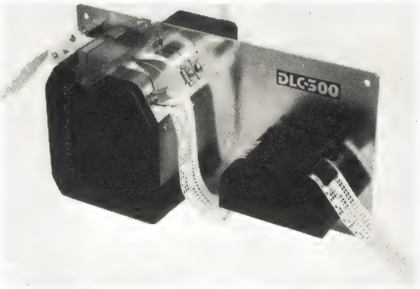
CIRCLE NUMBER 89

Punch/reader mechanism builds into OEM systems

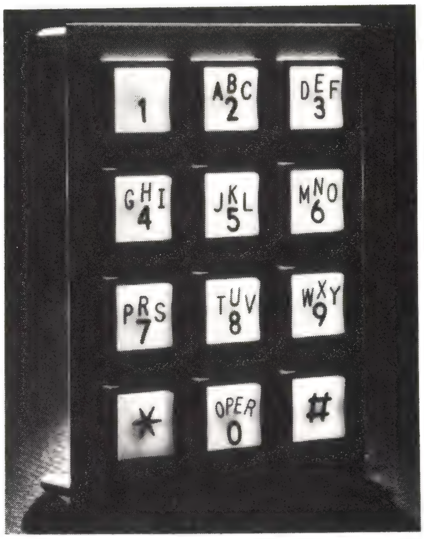


Drillick LaManna, 280 Midland Ave., Saddle Brook, NJ 07662. (201) 791-1414.

DLC 300, a punch and reader mechanism, mounts in OEM equipment. The unit operates at 30 characters/s and is driven by a single, synchronous motor; no stepping motors are required. The replaceable punch block handles Mylar. Tape is sensed by a matched phototransistor and LED. The reader includes a taut-tape feature.

CIRCLE NO. 371

Light shines through translucent keypads



Chomerics, 77 Dragon Ct., Woburn, MA 01801. (617) 935-4850. From $3.75 to $5.35 (1000 qty).

Translucent, sublimated keytops on ET Short Stroke keypads permit backlighting. The keys use a sublimated legend, transferred directly into their surface, to provide durability and wear resistance. The keyboard, using screened Mylar membrane technology, provides a crisp, tactile feel. The transparent membrane circuit and plastic backer allow good light transmission to the translucent keytops.

CIRCLE NO. 372

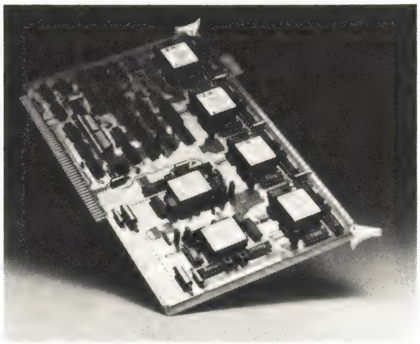
μC boards function in multicard systems

Synertek Systems, 150 S. Wolfe Rd., Sunnyvale, CA 94086. (408) 988-5600. $369 (MBC010); $495 (MBC020).

Two microcomputer boards, MBC010 and MBC020, operate in multiple-card systems using the Motorola EXORciser bus. MBC010 uses a 6500 or 6800 microprocessor and provides fully buffered data and address lines, 1024 bytes of static RAM and four ROM/EPROM sockets for 2716 or 2732-type devices. Communications includes 16 programmable I/O lines, 4 programmable control lines and two 16-bit programmable binary counter/timers. MBC020 includes all the features of the MBC010 plus a complete video section. The board supplies 25 lines of 80 characters and can accept a light-pen input. Both boards operate at serial data rates of up to 19,200 baud. TTL and RS232 interfaces are available.

CIRCLE NO. 373

Bubble board maintains nonvolatile storage

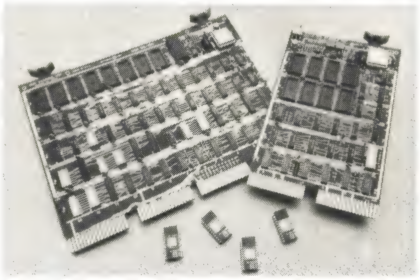


Texas Instruments, P.O. Box 225012, M/S 308, Dallas, TX 75265. (214) 238-2011. $775 to $1535; 4 wks.

A TM990-compatible board, TM990/210, stores up to 69 kbytes of nonvolatile magnetic bubble memory. The board has all necessary support circuitry for the bubble devices. Two, four or six 92-kbit TIB0203 bubble memories can be used for 23, 46 or 69 kbytes. Data transfers are via a memory-mapped mode. Transfers can be single or multipage. Access time is 4 ms; data transfer rate, 45 kbits/s. Power supply requirement is 5 and ±12 V.

CIRCLE NO. 374

Modules give computers on-board programming



MDB Systems, 1995 N. Batavia St., Orange, CA 92665. (714) 998-6900. $495 (MLSI-MRV-004); $995 (MDB-MR-004); 4 wks.

Plug-in modules for DEC PDP-11 and LSI-11 computers extend PROM programming capability. The computer, rather than an off-line device, can be used to burn PROMs on-line. Results can be tested, compared and executed immediately. MDB-MR-004 accommodates 2716 and 2732 UV-eraseable memories. The module requires one quad slot in the PDP-11 chassis. MSLI-MRV-004 is a dual module for an LSI-11 computer. It accepts 2716 and 2758 UV EPROMs.

CIRCLE NO. 375

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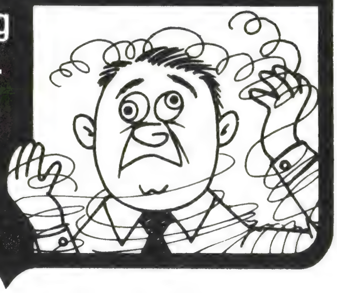
PRESSURE-SENSITIVE COPPER Design Products



If you're still prototyping with the old, familiar wire wrapping techniques, now's the time to join the growing number of professionals using the new QUIK-CIRCUIT Pressure-Sensitive COPPER Design System for PC prototyping or on-the-spot PC board repair. With QUIK-CIRCUIT's state-of-the-art system, you get *everything* you need to build reliable PC board prototypes or make repairs WITHOUT artwork, wire wrapping, photography, screening or etching.

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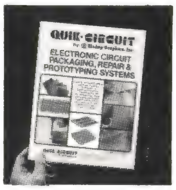

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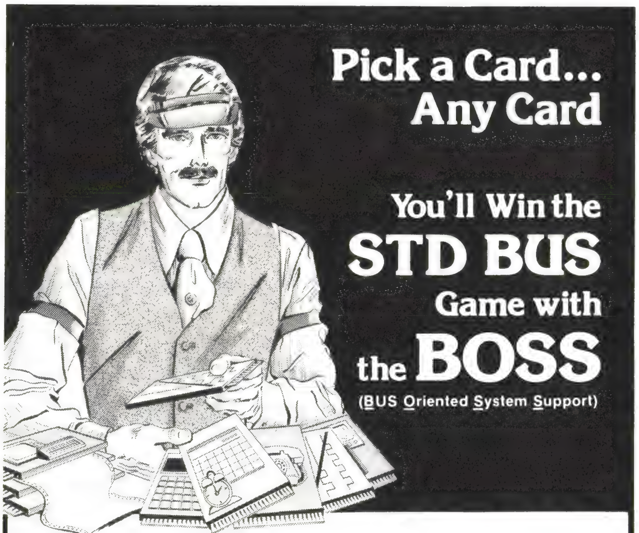
CIRCLE NUMBER 93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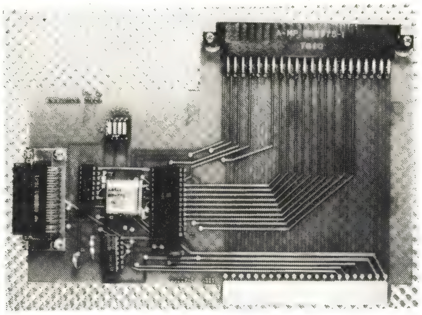
CIRCLE NUMBER 94

Interface opens RS232 world to AIM/KIM/SYM μCs



Fobel Enterprises, 552 E. El Morado, Ontario, CA 91764. (714) 984-8871. $69.95 (kit); $84.95 (assembled).

A programmable interface card allows connection of any RS232 device to an AIM, KIM or SYM microcomputer. Word lengths and baud rates are programmable. Features include odd/even parity generation and detection, serial echo mode, half and full duplex operation, parity, framing and overrun error detection and 1, 1-1/2 and 2 stop bits. A DB-25 connector is used. An additional connector provides for expansion.

CIRCLE NO. 376

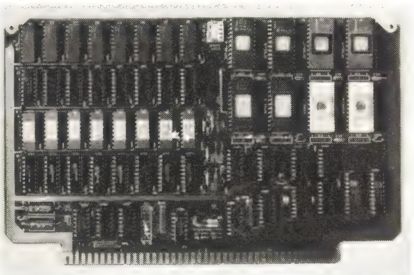
Parallel interface adds 64 lines to LSI-11 μCs

Digital Equipment, 129 Parker St., Maynard, MA 01754. (617) 897-5111. $420.

A high-density, parallel interface, DRV11-Q, adds 64 I/O lines to LSI-11/23 and LSI-11/2 microcomputers and their packaged counterparts, the PDP-11/23 and PDP-11/03. The 8.9 × 5.2-in. module uses a programmable interrupt structure with bit interruptability on up to 16 lines. The 64 lines are organized into four ports. Data line direction for each port is program selectable, requiring no hardware alteration. Up to 16 processor interrupts can be chosen—bit interrupts on 16 data lines, or four I/O interrupts (one per port) and 12-bit interrupt lines. Interrupt vectors are set under program control. Interrupts within the module can be programmed for fixed or rotating priority. The DRV11-J is suited for sensor I/O applications, such as chemical process and automatic test stand monitoring and control, where real-time response is necessary. The board can also be used as a general-purpose interface to custom devices.

CIRCLE NO. 377

Single board contains RAM/EPROM for 6800 μP



Phoenix Digital, 3027 N. 33rd Dr., Phoenix, AZ 85017. (602) 278-3591. From $450.

A single-card memory system, PCM 16-32, contains 16-k RAM and 32-k EPROM and/or ROM. The board is fully compatible with M6800, 6801, 6802, 6809 and 650X series devices. RAM can be expanded in 4-k block increments to a full 16-k. EPROM and ROM expand from 2-k to 16-k with 2716 memories and from 4-k to 32-k with 2732 or 2532 devices. RAM is protected during system initialization by on-board power-on reset circuitry. Separate power busing to each 4-k block of RAM allows easy provisioning for standby or power fail-safe requirements.

CIRCLE NO. 378

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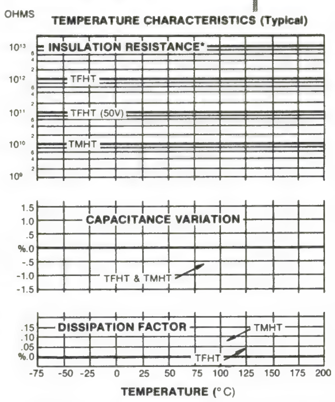

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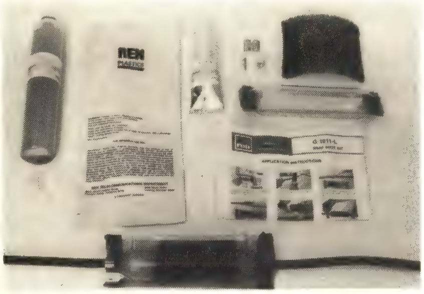
CIRCLE NUMBER 96

Kit prepares and encapsulates splices

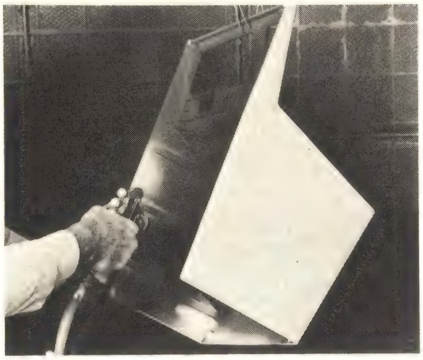


CIBA-GEIGY Telecommunications, 5250 Fulton Industrial Blvd., Atlanta, GA 30336. (404) 696-6400

A materials kit, G1011-L, contains everything needed to encapsulate plastic-insulated cable splices. The kit includes a two-component encapsulating compound which sets in 3 to 5 minutes. A splice-centering foam assures complete coverage around the splice. A closure, made of a transparent material, allows visual inspection of wire work before and during encapsulation.

CIRCLE NO. 379

Shielding liquid spray-coats plastics

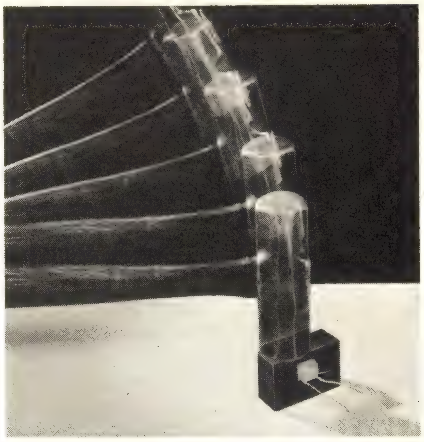


Metex, 970 New Durham Rd., Edison, NJ 08817. (201) 287-0800.

A dispersed-nickel conductive coating, Xecote, sprays on plastic enclosures for effective EMI/RFI shielding. The liquid adheres to a wide variety of surfaces including acrylics, polycarbonates, polyphyenylene-oxide, fiberglass, sandblasted steel and other plastics and metals. Surface resistivity is 1 Ω/sq. Attenuation is 45 dB at 10.3 GHz; 53 dB at 450 MHz for a 0.002 to 0.003-in. dry coating. One gallon of Xecote covers 270 ft^2.

CIRCLE NO. 380

Epoxy casting resin takes hard knocks



Emerson & Cuming, 869 Washington, St., Canton, MA 02021. (617) 828-3300.

Stycast 1426, a one-part, filled epoxy resin system, delivers high impact strength. Medium viscosity and short cure cycles at relatively low elevated temperatures (79 C) are added advantages. Viscosity is 70,000 centipoises at 25 C; flexural strength, 15,500 lb/in.^{2}; compressive strength, 16,000 lb/in.^{2}. Dielectric strength is 480 V/mil; volume resistivity, more than 10^{14} Ω-cm at 25 C.

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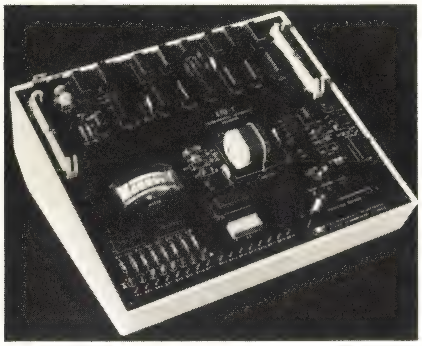
CIRCLE NUMBER 98

Interface designer teaches analog/μC interfacing



E&L Instruments, 61 First St., Derby, CT 06418. (203) 735-8774.

An interface designer, EID-1, teaches and demonstrates the principles of analog interfacing with a microcomputer. The unit connects directly to the MMD-1 or MMD-2 training and design microcomputers and is readily adaptable for use with other 8080-based microcomputers. I/O signals, representing such variables as light intensity, speed, temperature and position, can be provided or simulated by built-in components. Analog signals, converted to digital input, can be displayed on a LED readout. Digital signals can be generated on-board. Computer output can be converted to analog signals for meter display or motor speed control. The EID-1 trainer is available in kit or assembled form.

CIRCLE NO. 382

Computer uses fast CPU for scientific work

Data General, Rte. 9, Westboro, MA 01581. (617) 366-8911. Approx. $16,500 to $88,000; 13 wks.

A fast single-board CPU, enhanced by a memory pre-fetch processor (PFP), extends the computational performance of the ECLIPSE S/140 scientific computer system. Single-board design allows system expansion through a 16-slot chassis. PFP speeds execution time by reducing CPU latency. Microprogrammed implementation uses a 56-bit microword, permitting parallel overlapped CPU operations to be executed every microcycle for increased system throughput. A basic S/140 system comes with 128 kbytes of MOS memory with standard error checking and correction (ERCC). Memory expands to 1 Mbyte. The system is supported by all ECLIPSE operating systems, languages and utilities.

CIRCLE NO. 383

Pascal goes to work on industrial jobs

Process Computer Systems, 750 N. Maple Rd., Saline, MI 48176. (313) 429-4971.

A version of Pascal, storable in PROM, extends the block-structured language to process control, materials handling, machine control and source data acquisition applications. Industrial Pascal saves the cost of floppy disk storage equipment at each target or remote location. The software features n-dimensional arrays, high-speed floating-point math, integers, Boolean logic (AND, OR, XOR, NOT), a modified "P-code" pseudo machine and flexible data presentations. Users benefit from fast development time, direct I/O access, a structure language, multitasking, easy loading, less hardware and on-line graphics.

CIRCLE NO. 384

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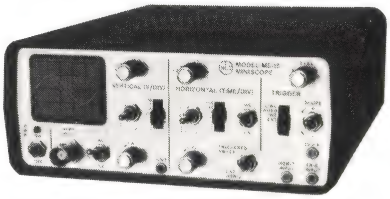

MS-15 $349.80
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- Line synchronization mode.
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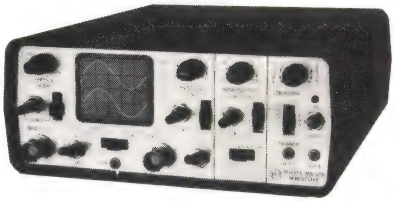

MS-215 $465.45
15 MHz — Dual-Trace
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- Line synchronization mode.
- Power usage—<15 W.
- Battery or line operation.
- 2.9" H x 6.4" W x 8.0" D.

MS-230 $598.15
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- Line synchronization mode.
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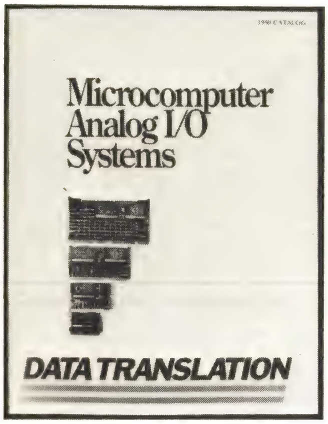
CIRCLE NUMBER 74

New Literature



μC analog I/O systems

Microcomputer Analog I/O Systems, 124 pages, details applications, specifications, user instructions and pricing for more than 80 product families. Data Translation, Natick, MA

CIRCLE NO. 385

Terminal strips

Strip-connector products for DIP and SIP packaged devices are detailed in a 16-page catalog. Samtec, New Albany, IN

CIRCLE NO. 386

Lasers and accessories

Scientific lasers and accessories are covered in a 16-page catalog. Spectra-Physics, Laser Instruments Div., Mountain View, CA

CIRCLE NO. 387

Thick-film materials

A 12-page brochure covers thick-film materials and systems for hybrid microelectronics and electro-optics applications. Cermalloy, Cermet Div. of Bala Electronics, W. Conshohocken, PA

CIRCLE NO. 388

Test instruments

A 24-page catalog provides specifications of test instruments and accessories. Amprobe Instrument, Lynbrook, NY

CIRCLE NO. 389

Jacketed flat cable

Flat cable for external interconnection of electronic equipment is described in a four-page catalog. The catalog lists cable specifications and properties as well as selected applications. Brand-Rex, Willimantic, CT

CIRCLE NO. 390

Lugs and clips

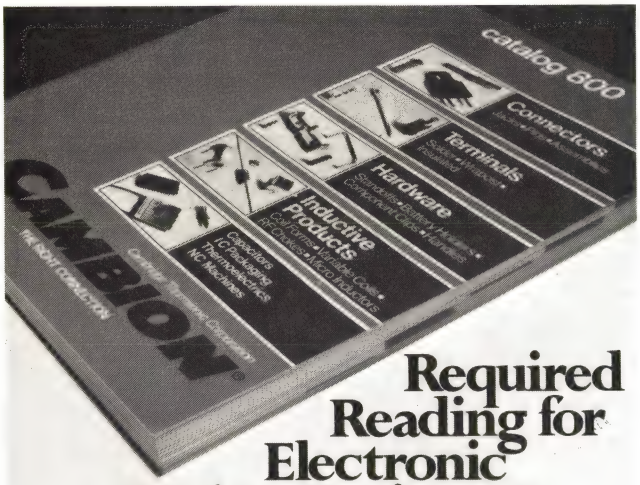
A 54-page guide features connectors, solder lugs, clamps, terminals and clips. Dimensional illustrations and engineering drawings to exact size are included. Zierick Manufacturing, Mount Kisco, NY

CIRCLE NO. 391

Optical encoders

Absolute and incremental optical encoders are detailed in easy-to-read data sheets. Descriptions, features, ordering information, options, electrical, mechanical and military specifications, as well as outline drawings, are included. Itek Measurement Systems Div., Newton, MA

CIRCLE NO. 392



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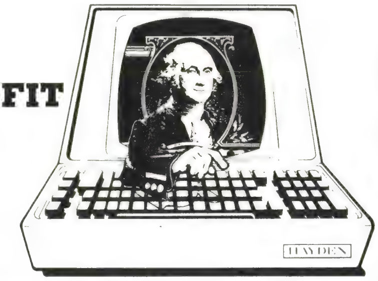
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CIRCLE NUMBER 102

(continued from page 161)

Magnetic cores

A 62-page PQ core bulletin and applications data book helps power supply designers to develop higher performance and lower cost switching supplies. TDK Corp. of America, El Segundo, CA

CIRCLE NO. 393

Coaxial adapters

Specifications, outline drawings, graphs and price information for coaxial and waveguide adapters, covering dc to 26.5 GHz, are presented in a four-page catalog. The Narda Microwave Corp., Plainview, NY

CIRCLE NO. 394

Wire-wrapping tools

Wire-wrapping tools and other electronic assembly tools and parts are featured in a 20-page catalog. Specifications and prices are included. O.K. Machine and Tool, Bronx, NY

CIRCLE NO. 395

Hose and couplings

A 56-page catalog describes Synflex hose, couplings and accessories for fluid power systems. The catalog includes a brief summary of thermoplastic hose technology. Eaton Corp. Synflex Div., Mantua, OH

CIRCLE NO. 396

Computer system

A powerful computer system, the V/32, that executes industry-standard 370 software without any reprogramming is described in a brochure. Two Pi Corp., Santa Clara, CA

CIRCLE NO. 397

Data logger

A data sheet describes the Micro280 data logger, an intelligent terminal controller. Micom Systems, Chatsworth, CA

CIRCLE NO. 398

Data-acquisition products

Transducers, amplifiers, filters, MUXs, references and a/d and d/a converters are described in a 28-page catalog. National Semiconductor, Santa Clara, CA

CIRCLE NO. 399

Solenoids

Linear high-performance solenoids are described in a 24-page handbook/catalog. The handbook section presents practical examples of solenoid selection in a problem/solution format. Electroid, Springfield, NJ

CIRCLE NO. 404

Minicomputers

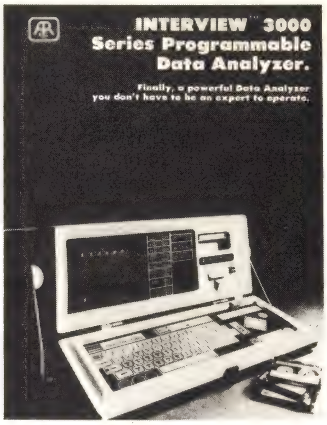
A 16-page minicomputer catalog describes the firm's hardware and software line. The catalog contains product photographs, configuration charts, pricing and ordering instructions. Educational Data Systems, Irvine, CA

CIRCLE NO. 405

Portable recorder

The BM-12 Standard, the smallest standard portable cassette in Sony's line, is highlighted in a brochure. Specifications and optional accessories are included. Sony Information Center, Business Products Div., Trenton, NJ

CIRCLE NO. 406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you don't have to be an expert to operate.

Data analyzers

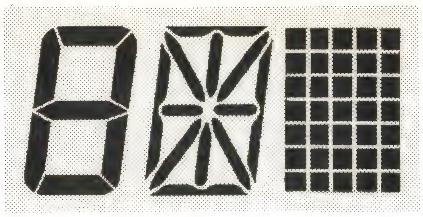
The 3000 Series programmable data analyzers are described in a catalog. Atlantic Research, Alexandria, VA

CIRCLE NO. 407

Pressure transducers

Dynamic, electrical, environmental and physical data on a series of miniature metal diaphragm pressure transducers are provided in a 12-page catalog. Outline drawings and schematics are included. Kulite Semiconductor Products, Ridgefield, NJ

CIRCLE NO. 408



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The displays are competitively priced and yet are reported to incorporate state-of-the-art features including: extended temperature range, reduced response time, high visibility, and long life. Color Reflectors, which have good lamp effects, are also available.

For more information, contact:

Seiko Instruments, Inc.
2990 W. Lomita Blvd.
Torrance, CA 90505
213/530-3400

CIRCLE NUMBER 106

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Electronic Design's

RECRUITMENT SECTION

Application Notes

Fiber optics

"Everything You Need in Optical Communications" helps designers who want to select components to construct fiber-optic systems or those who want to upgrade an existing communications system. Valtec, West Boylston, MA

CIRCLE NO. 409

Pneumatic actuators

The function of the pneumatic actuator as a positioning, dispensing, deposition, vacuum-sensing, mixing and pumping device for providing motive force in applications such as computer peripherals, medical equipment and semiconductor processing equipment is explained in a bulletin. Airpot Corp., Norwalk, CT

CIRCLE NO. 410

Relays

How bounce-free mercury film Series W relays used in a modem circuit board permit the board to be mounted in any position is described in a four-page bulletin. Fifth Dimension, Princeton, NJ

CIRCLE NO. 411

Quartz crystals

The *Quartz Technology Manual*, 150 pages, contains comprehensive information on quartz crystal design and specification. Sentry Mfg. Co., Chickasha, OK

CIRCLE NO. 412

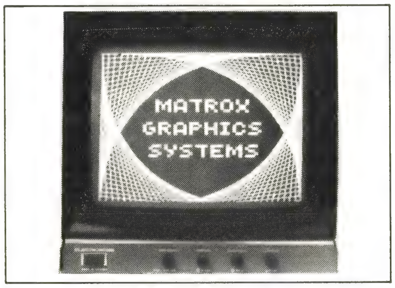
Thermistors

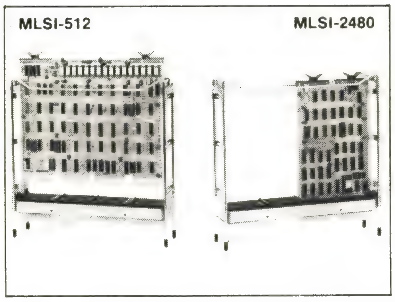
The Capsule Thermistor Course Booklet, 24 pages, gives a brief, technical insight into the What, Where and How's of thermistor sensors and sensor assemblies for use in temperature measurement, indication and control applications. Fenwal Electronics, Framingham, MA

CIRCLE NO. 413

matrox

PDP-11 and LSI-11 bus displays





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Issue Date	Closing Date	Mailing Date
February 1	**January 4**	January 18
February 15	**January 18**	February 1
March 1	**February 1**	February 15
March 15	**February 15**	February 29
March 29	**February 29**	March 14
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Senior Electronics Design Engineer

BSEE and 3 years experience. Wideband analog design, Phase-lock-loop experience, or TTL, CMOS, and CMOS Digital Design experience.

Senior Engineer

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Cable Engineer

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(3) radiofrequency systems including stabilized oscillators, rf amplifiers, broadband circuit impedance matching, cavity resonators, low power rf signal circuits, and rf scaler/counters. Frequency range of interest is 1 MHz to 1 GHz;

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- Familiarity with a variety of test instrumentation (oscilloscopes, waveform generators, pulsers, spectrum analyzers, rf test devices, reflectometers, etc.) for measurement and qualification of electronic devices under development.
- Design experience in one or more of the above technical specialities.
- Ability to interact effectively with other electronic engineers and with physicists to establish appropriate system and device parameters and to refine designs as development progresses.
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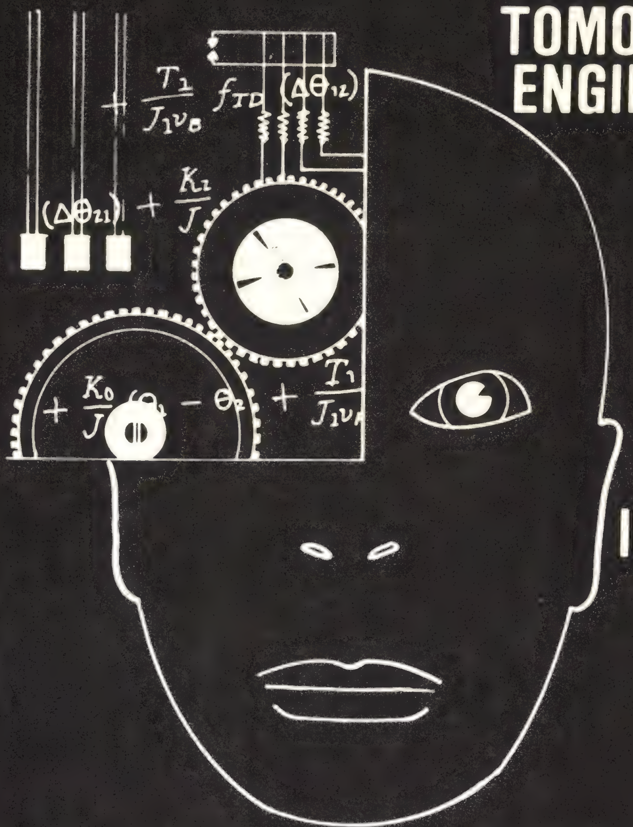

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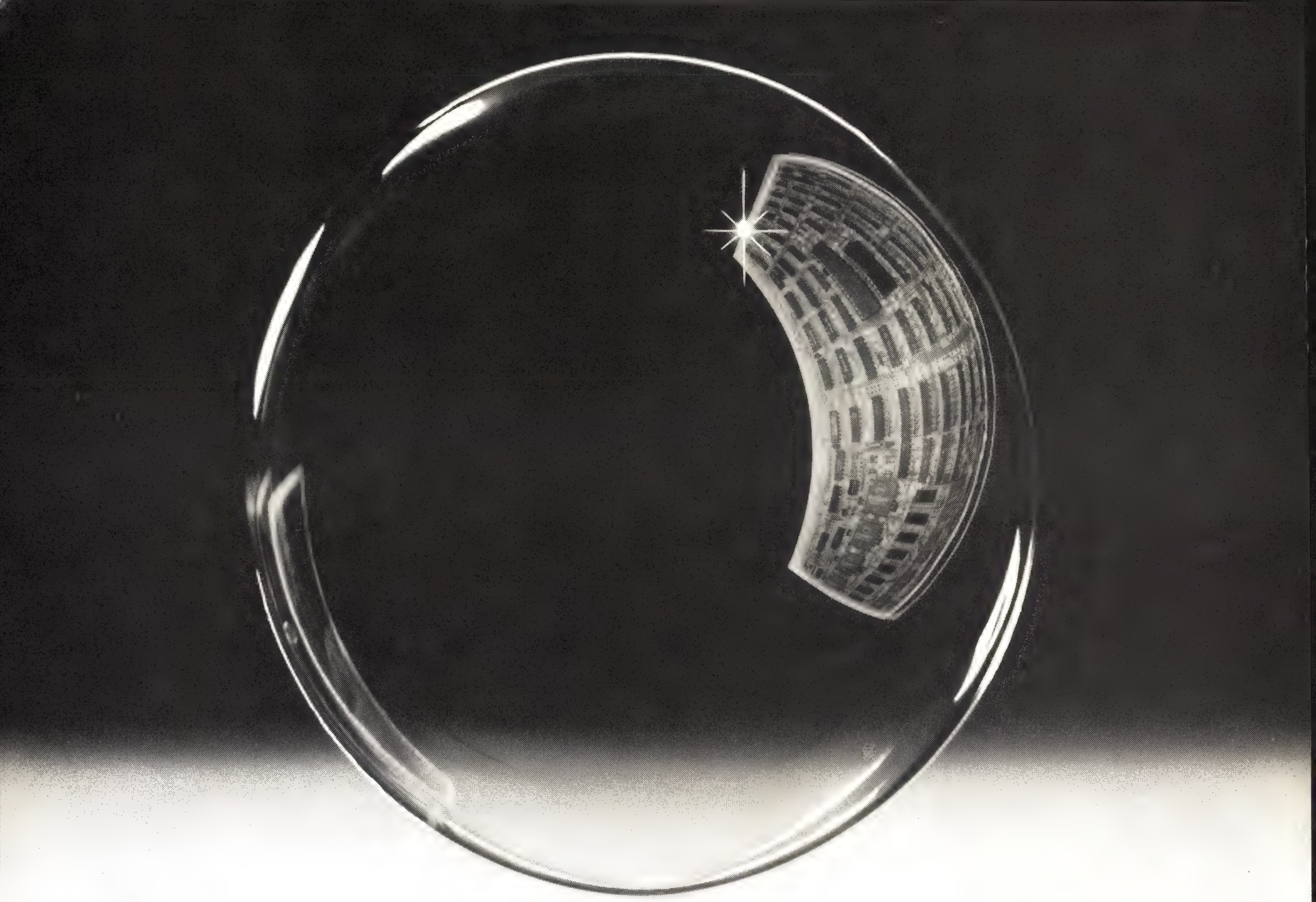

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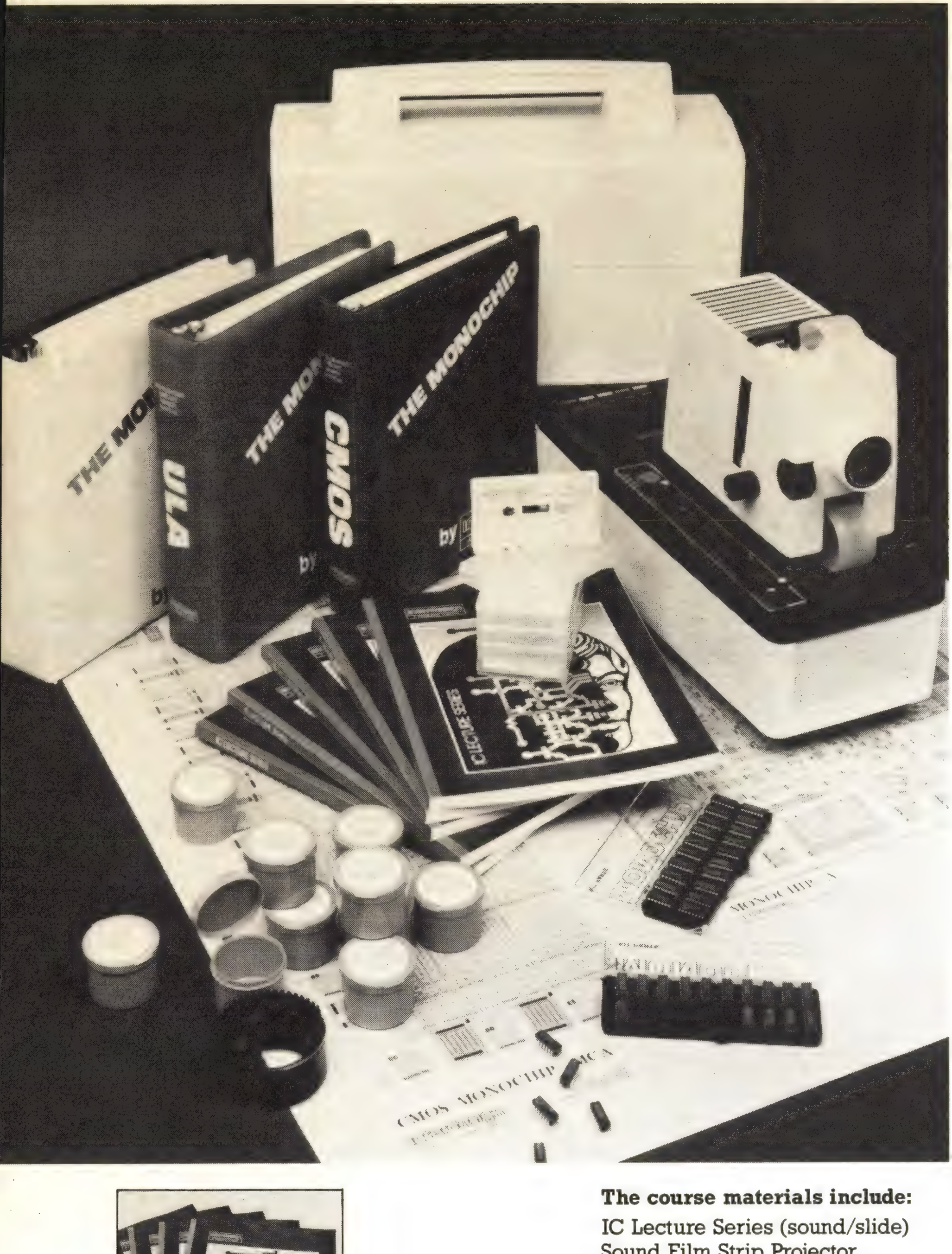

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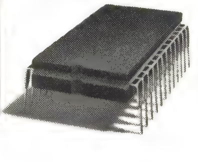

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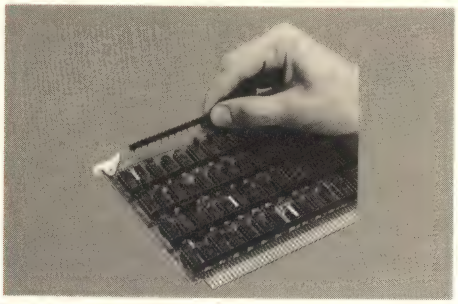

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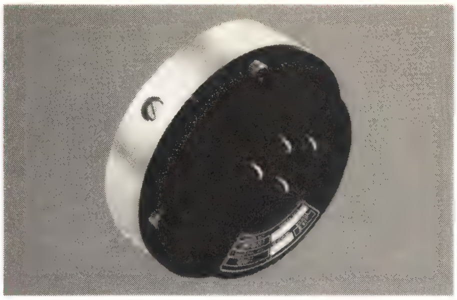
Q/PAC ELEMENTS 151



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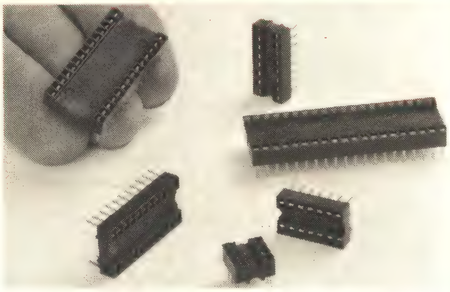

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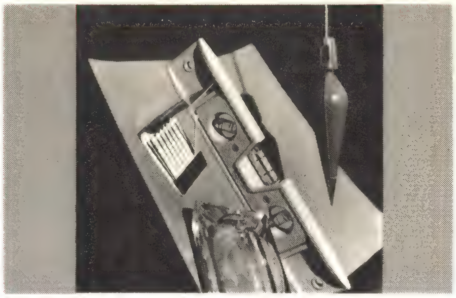

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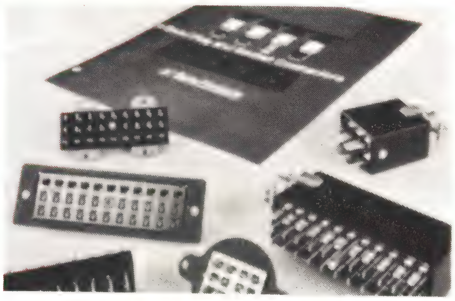

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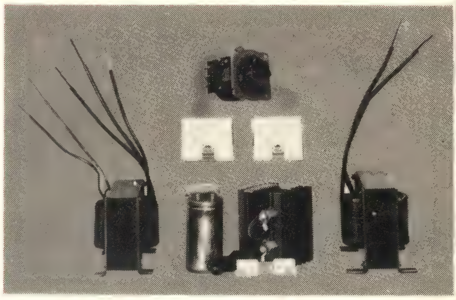

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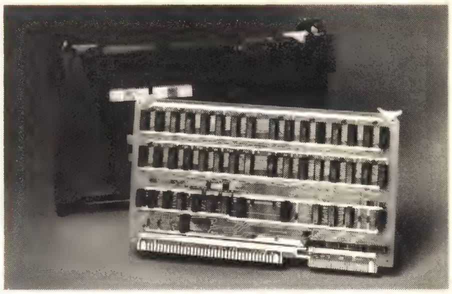

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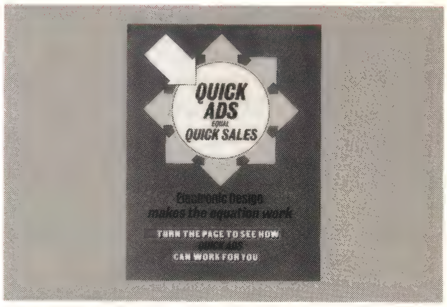
STATIC RAM 158



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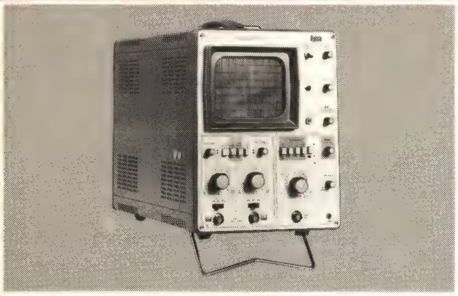

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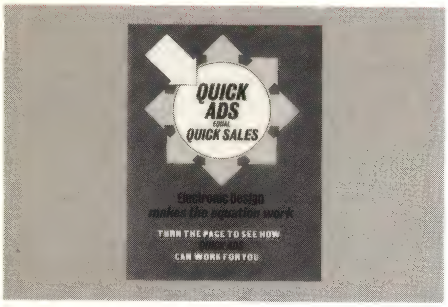

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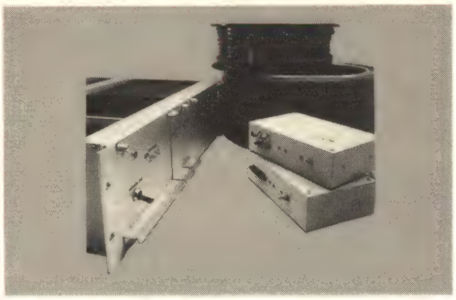

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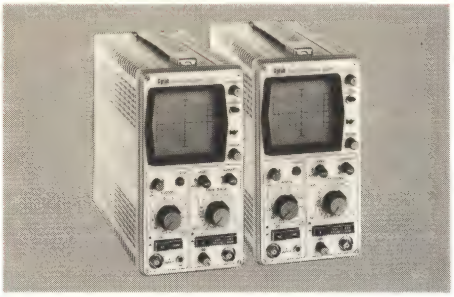
COMMUNICATION FIBEROPTICS **163**



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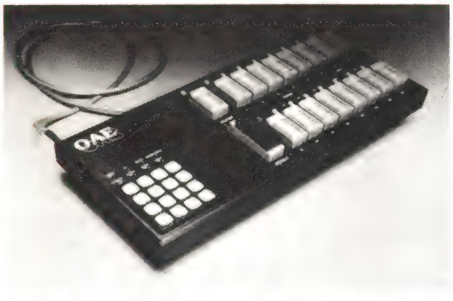

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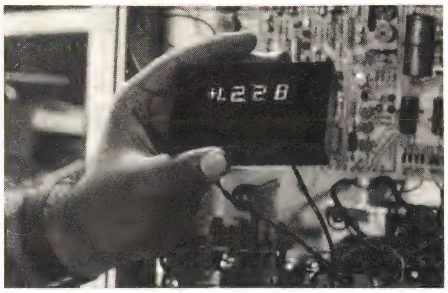

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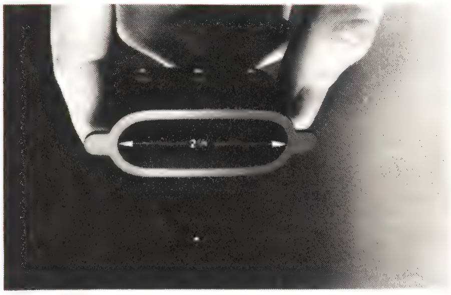
FLAT DPM MODEL 1021 **167**



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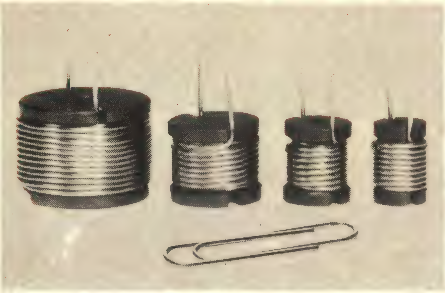

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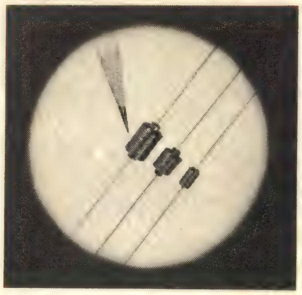

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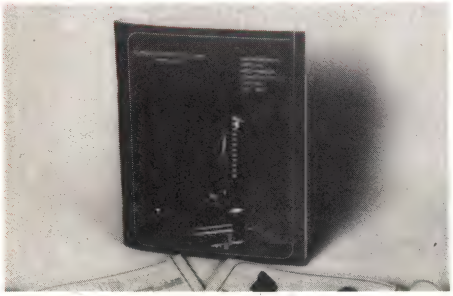

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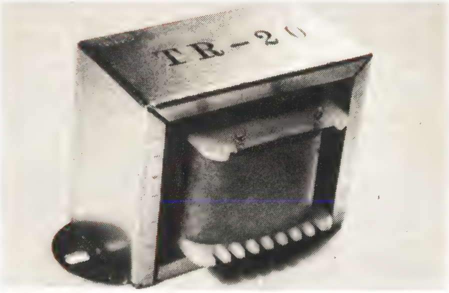

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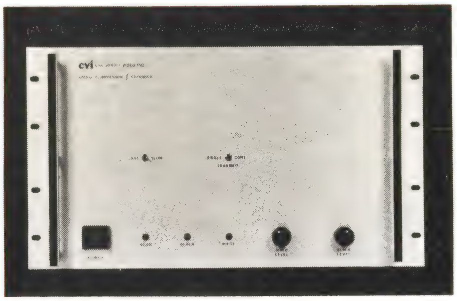

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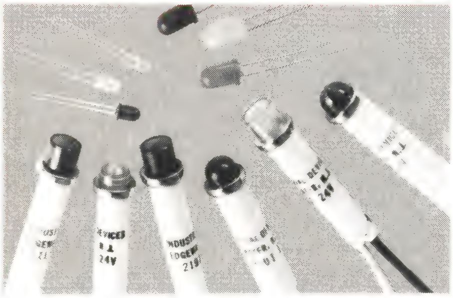

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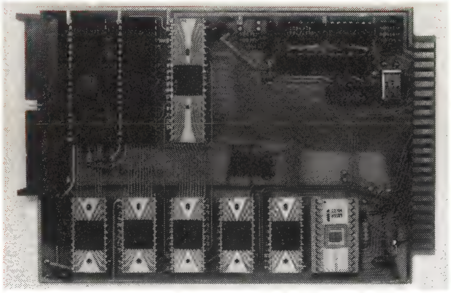

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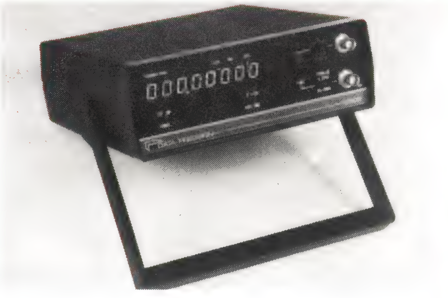

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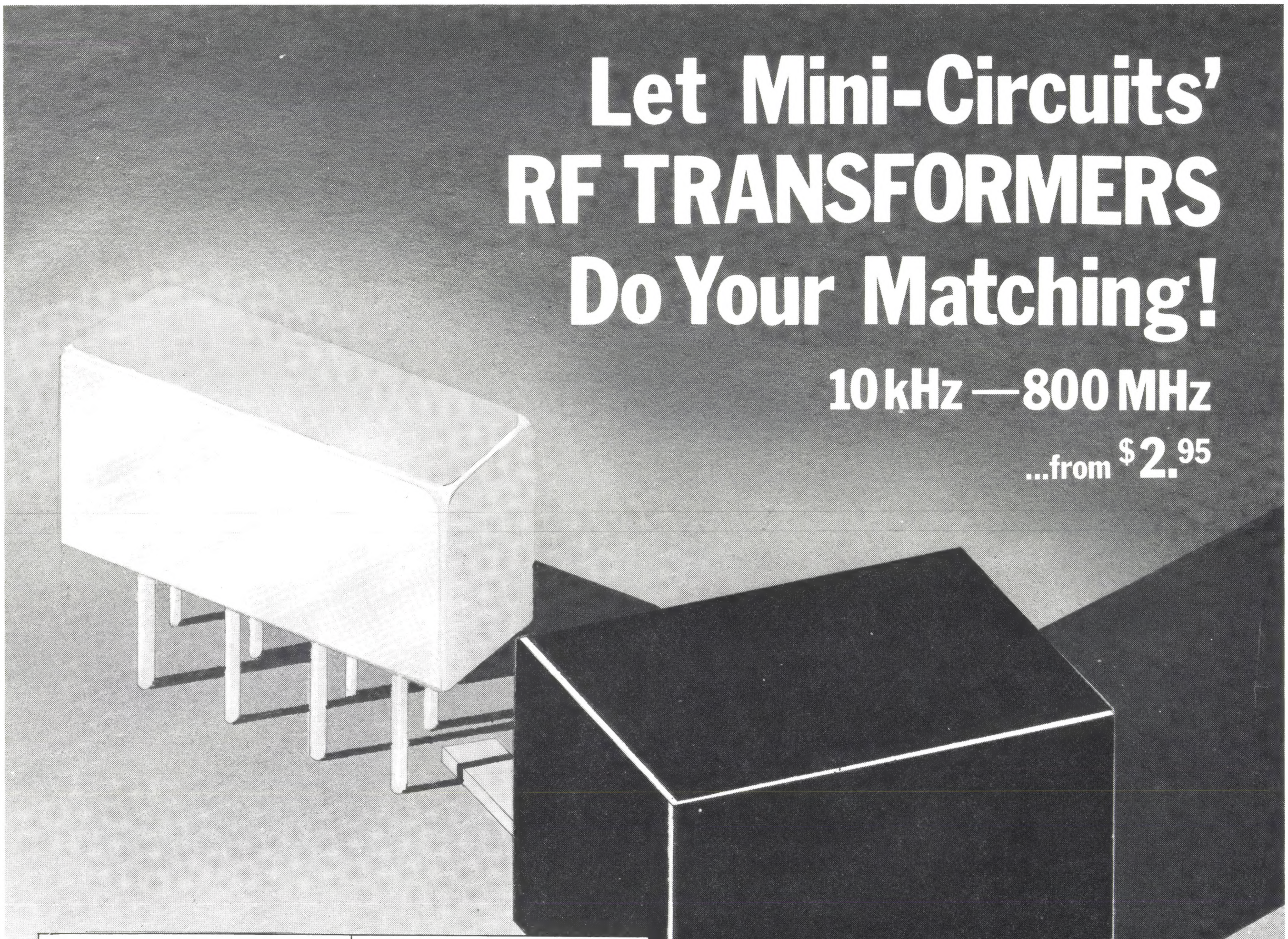

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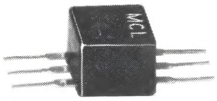

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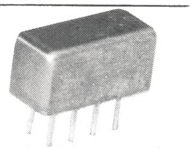

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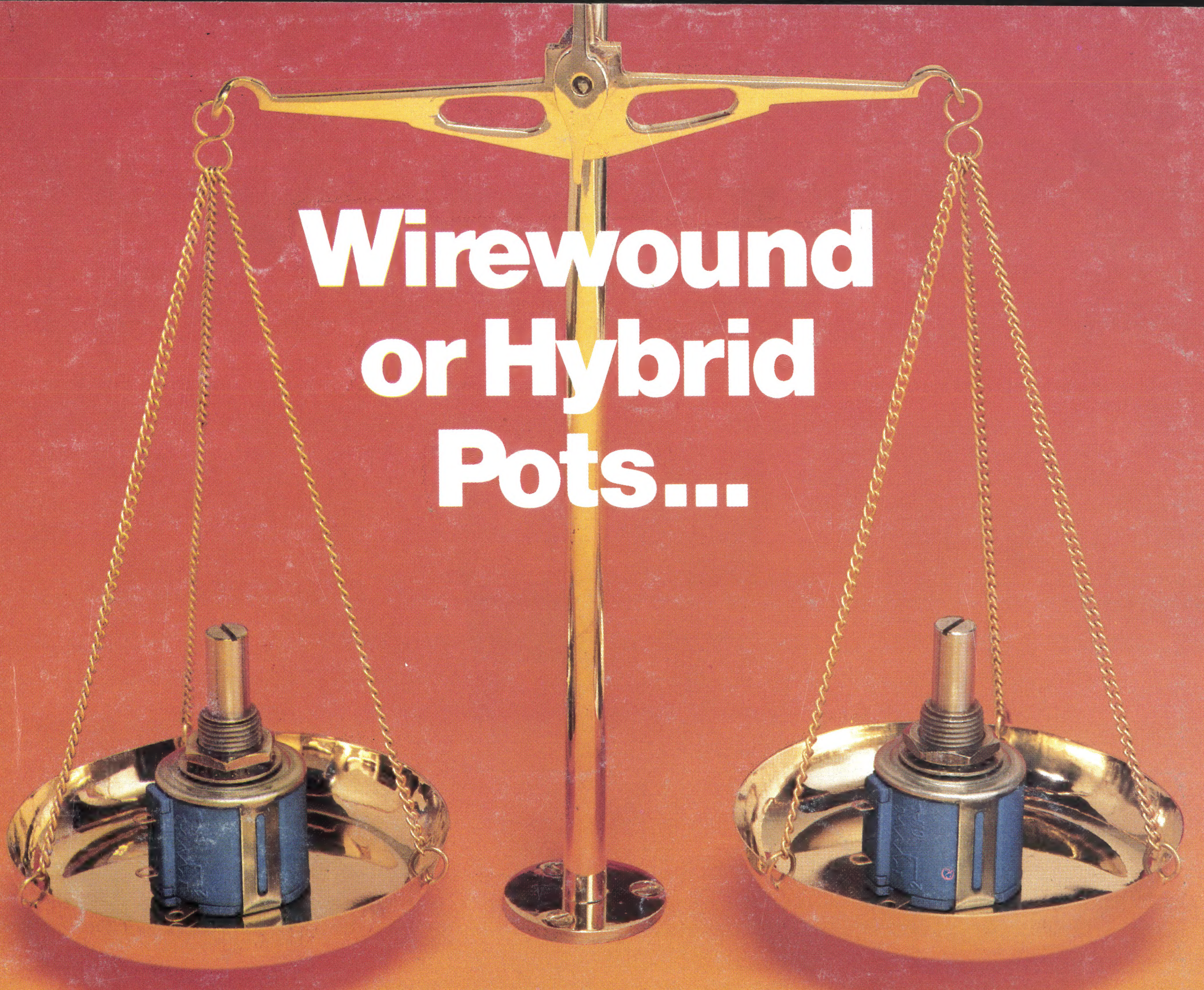

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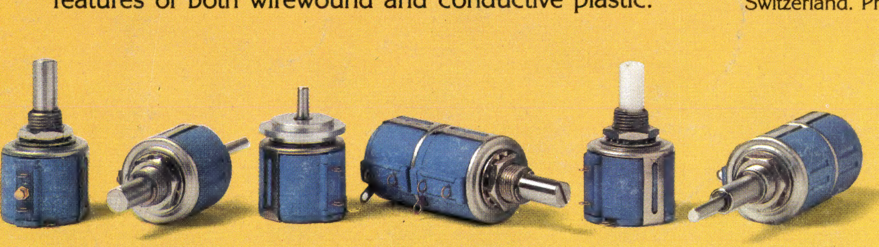

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